

Aim: To reset mixer information and passwords.

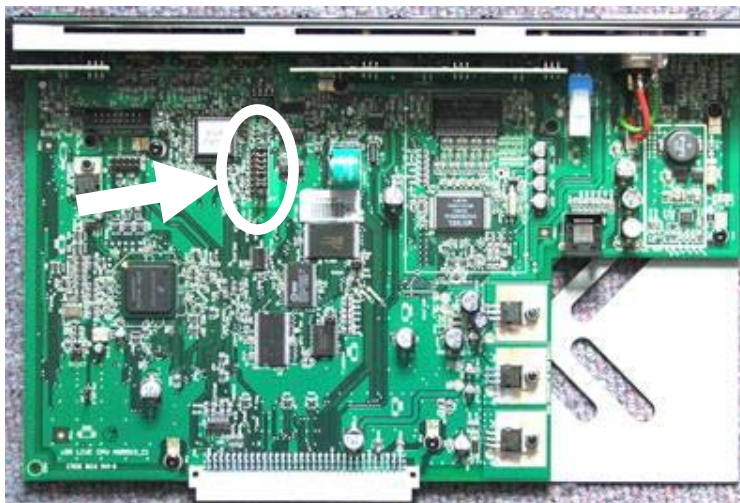
Tools: ☆ T10.  Module extraction tool

Requirements:

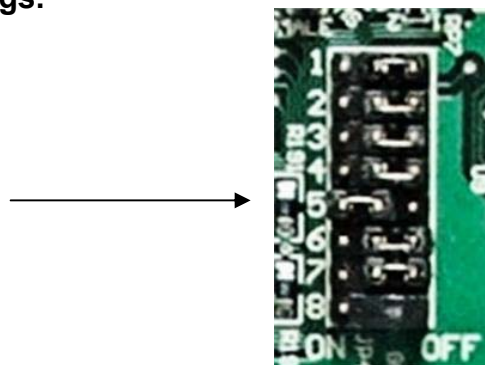
- Removal of iLive CPU module. Refer to iLive service document 2.08
- Removal of iDR10 CPU module. Refer to iLive service document 2.08

**Reset procedure**

1. Power OFF.
2. Remove CPU module. Refer to iLive service document 2.08
3. Locate jumper bank JP4. During normal operation, all jumpers should be OFF



4. Put appropriate jumper link to ON position. This picture shows J5 ON to reset mixer settings.



5. Replace CPU module.
  6. Power ON and allow unit to fully boot.
  7. Power OFF.
  8. Remove CPU module.
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9. Replace jumper link to OFF position.



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10. Replace CPU module.
  11. Power ON and allow unit to fully boot.
  12. The desired reset is now complete.
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The following page lists jumper function and memory locations.

## Jumper links

### **J5 Resets mixer settings**

- Processing - current settings [iDR10 CPU]
- Strip assignments [i-Live CPU]

### **J6 Clears all scenes** [Both i-Live and iDR10 CPU]

### **J7 Clears configuration sector**

- Input setup – mono and stereo channel settings [MixRack CPU]
- Mix configuration [MixRack CPU]
- Buss configuration [MixRack CPU]

#### Reset user profiles

User names

User passwords

User permissions

User default power-up scene

- IP address [Both i-Live and MixRack CPU]

### **J8 Reset user profiles. Up to** → **V1.32 J8 on the SURFACE CPU**

**V1.40** → **J8 on the MIXRACK CPU**

- User names
- User passwords
- User permissions
- User default power-up scene

## Memory location

**Scene** – Both MixRack and iLive. MixRack Settings stored in MixRack. Strip assignments, local mic pre and local digital source select are stored in iLive. Cleared by **J6**.

**Show** – Stored on SBC on compact flash or USB.

**FX** – Stored as Libraries on SBC compact flash or USB. Current settings saved in scene (see above).

**Permissions** –iLive – Flash (Config Sector) Cleared by **J8 OR J7** see notes above.

**Processing** – (Current Settings) Stored in battery backed SRAM – MixRack CPU PCB. Cleared by **J5**.

**User profiles** – iLive – Flash (Config Sector) Cleared by **J8 OR J7** see notes above..

**IP** – Both MixRack and iLive – Flash (Config Sector) Cleared by **J7**. Also on SBC compact flash.

**Event log** – Both MixRack and iLive in BB SRAM.

**Preferences.** Most are stored locally to the host they affect.

**Date/time.** MixRack and iLive, Clock Chip on CPU PCB. SBC compact flash. All set using SBC.

**Mix Configuration** – MixRack – Flash cleared by J7

**Bus Configuration** - MixRack – Flash cleared by J7

**Strip assignment** – iLive BBSRAM cleared by J5