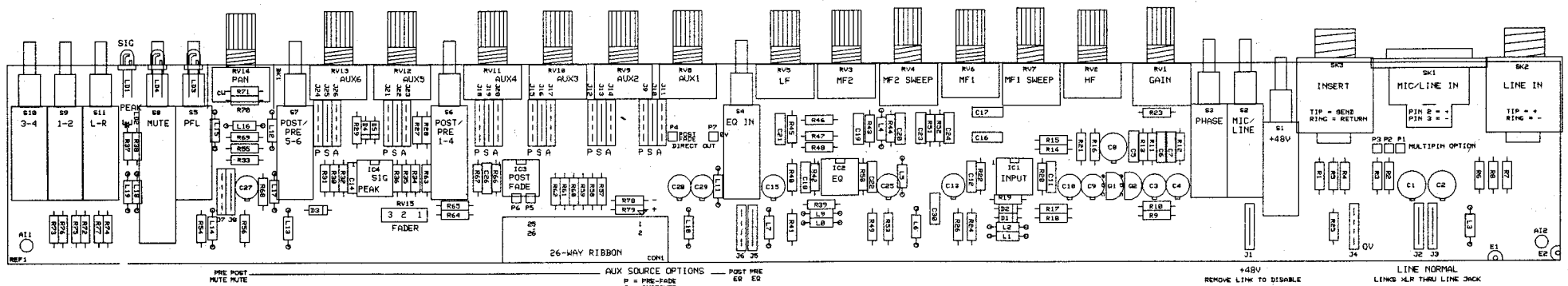
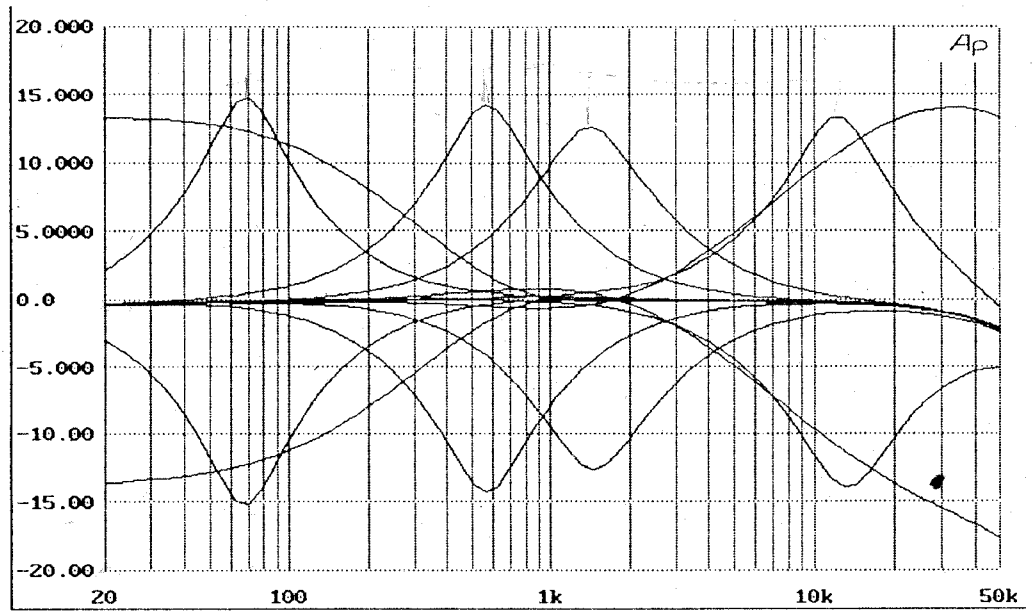
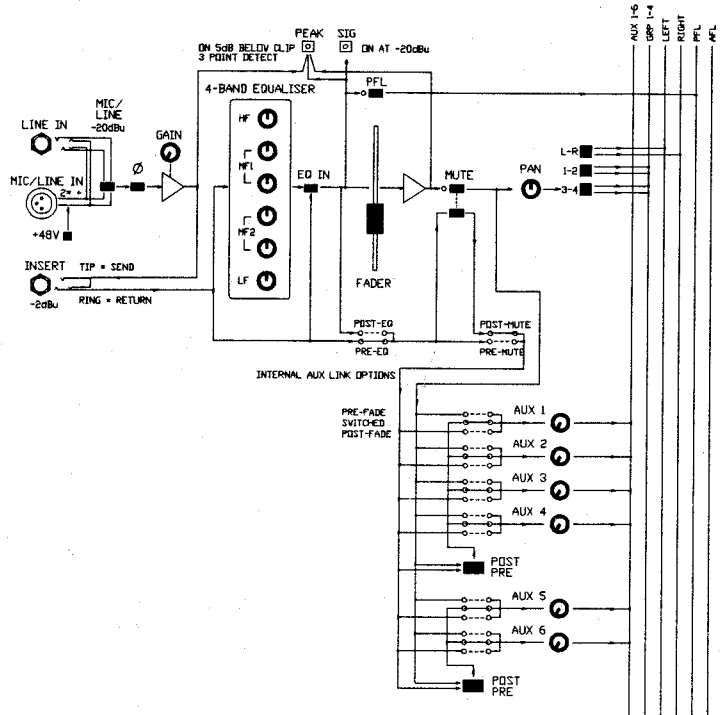
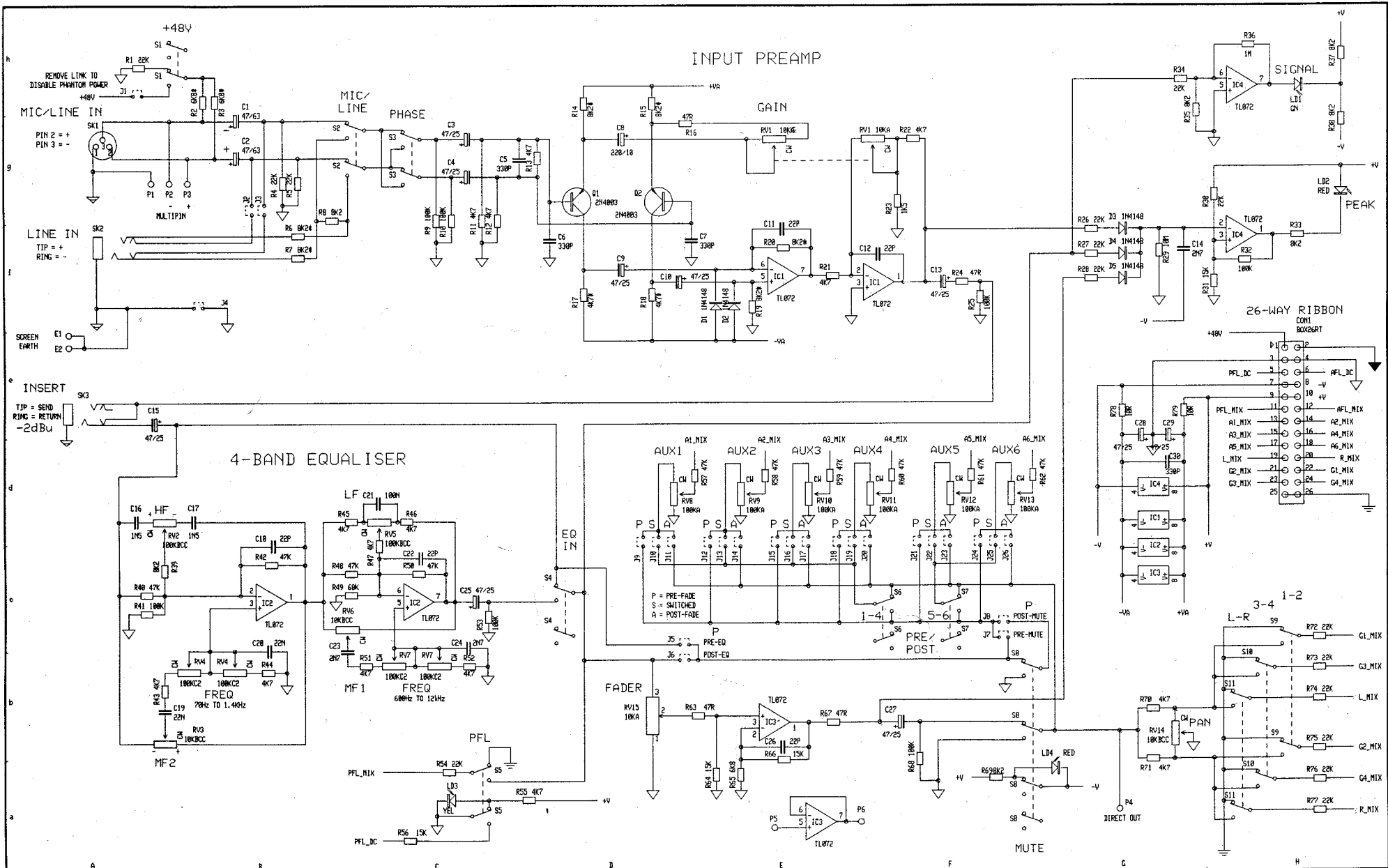


# EQUALISER



AUX SOURCE OPTIONS — POST PRE ER EQ  
 P = PRE-FADE S = SWITCHED A = POST-FADE  
 REMOVE LINK TO DISABLE LINE NORMAL LINKS -LR THRU LINE JACK



ISS.	REVISION	BY DATE	NOTES
P1	ORIGIN	CD 1-7-92	1. RESISTORS MARKED $\frac{1}{4}$ ARE 1/4
1	PRODUCTION	CD 30-8-92	ALL OTHERS ARE 5K 1/4W UNLESS OTHERWISE MARKED
			2. ELECTROLYTIC CAPACITORS ARE $\mu$ F-VOLTS

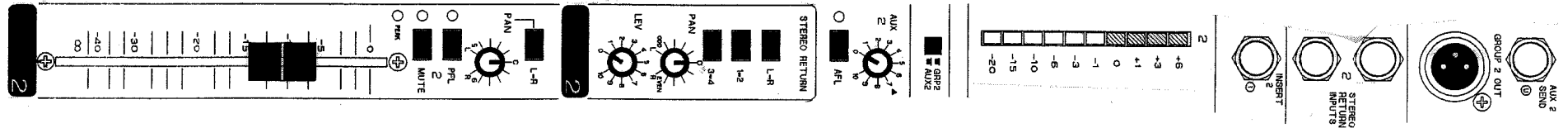
**INPUT**

UNIT TITLE  
**GL3**

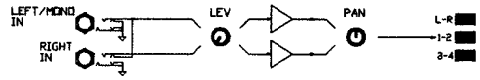
DRAWING TITLE  
**INPUT-4 CIRCUIT DIAGRAM**  
PCB TYPE AQ0321

MANUFACTURED IN ENGLAND BY  
**ALLEN & HEATH**

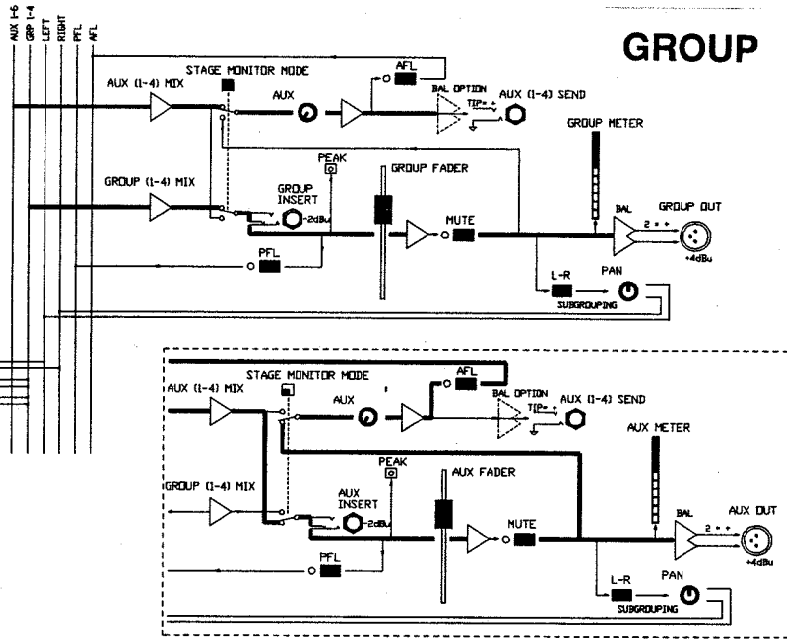
DRAWING No. **D176** ISSUE **1**



### STEREO RETURN



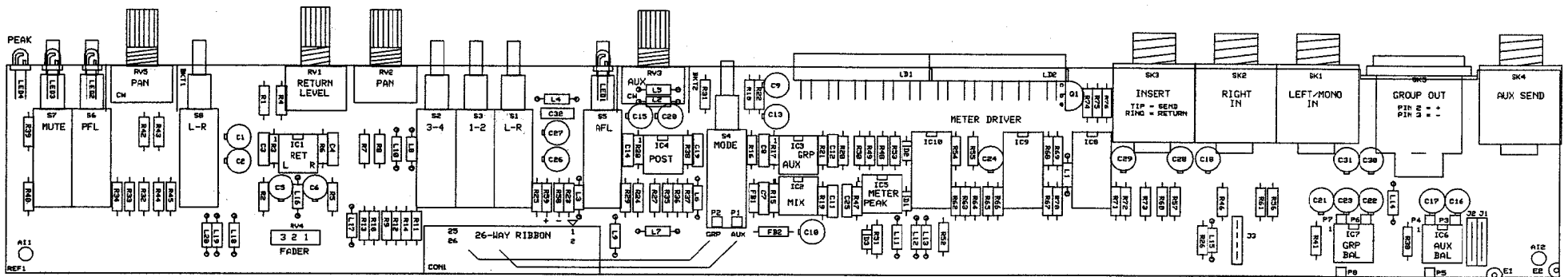
### GROUP

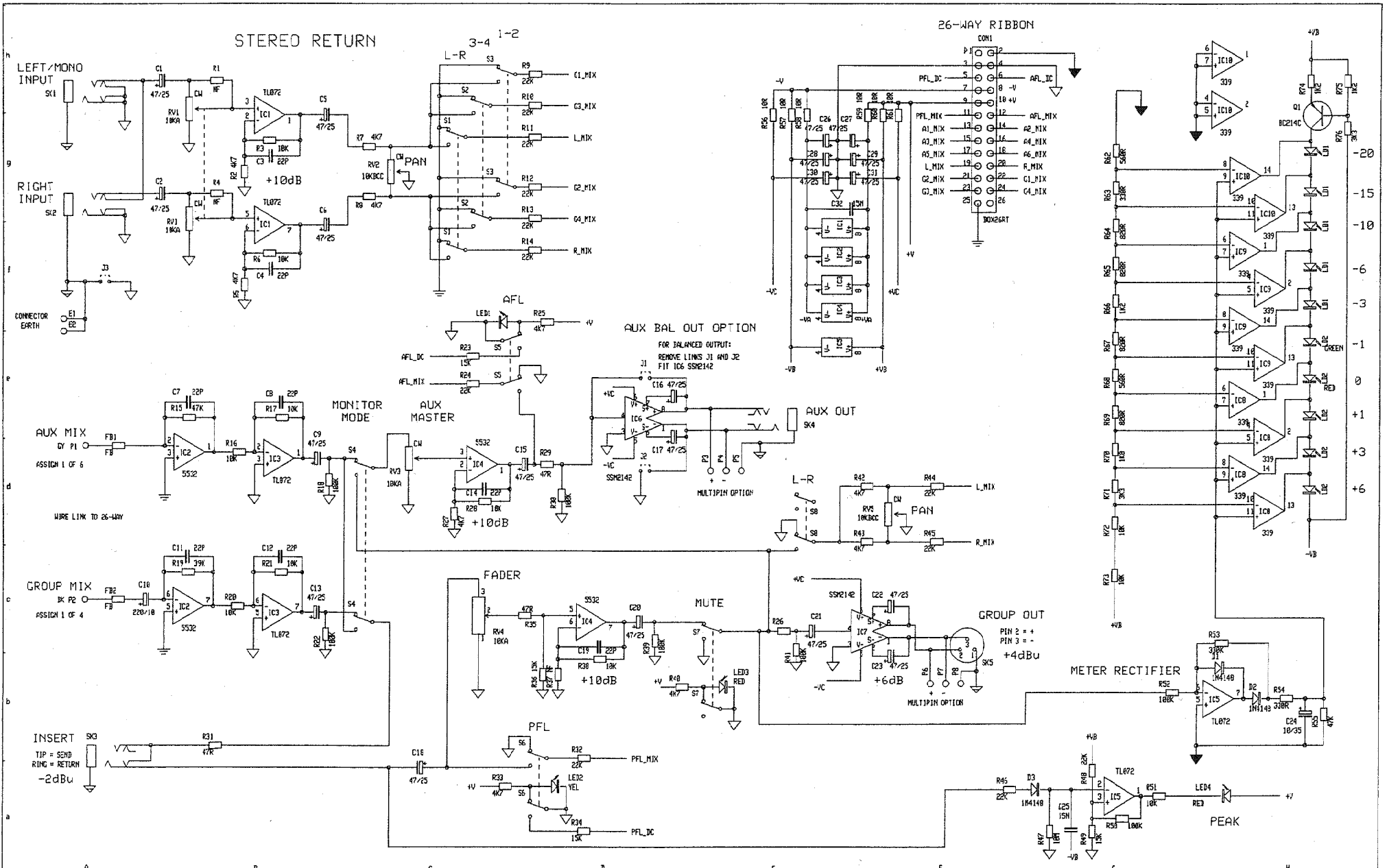


### GROUP MODE SWITCHING:

Here the upper block diagram shows the main signal path (in bold) optimised for F-O-H or conventional group/aux operation with the **MONITOR MODE** switch in the up position (flush with panel).

The lower (boxed) block diagram shows the signal path optimised for **STAGE MONITOR** operation with the **MONITOR MODE** switch pressed (to below panel). In this mode the **AUX MASTER** level control is used to adjust the **AFL** level used to set up the engineers **WEDGE MIX**. For single **AFL** monitoring this control should be set to its '0dB cal' mark.





ISS.	REVISION	BY	DATE
P1	ORIGIN	CD	17-7-92
1	PRODUCTION	CD	30-8-92
2	IC4 WAS TL072 R37 DELETED	DRP	8-12-93

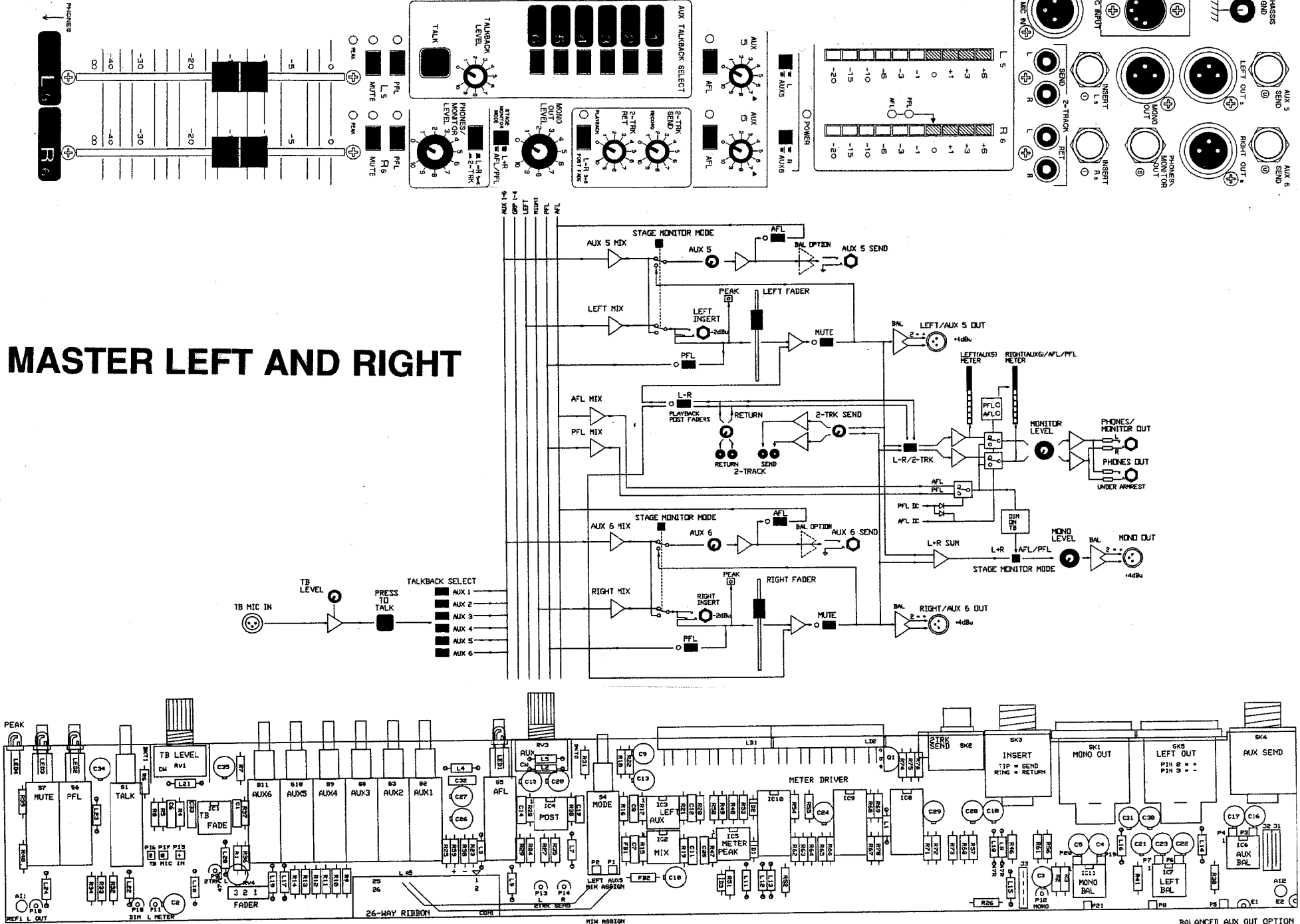
NOTES
1. RESISTORS MARKED * ARE 1% ALL OTHERS ARE 5% 1/4W UNLESS OTHERWISE MARKED
2. ELECTROLYTIC CAPACITORS ARE $\mu$ F/VOLTS

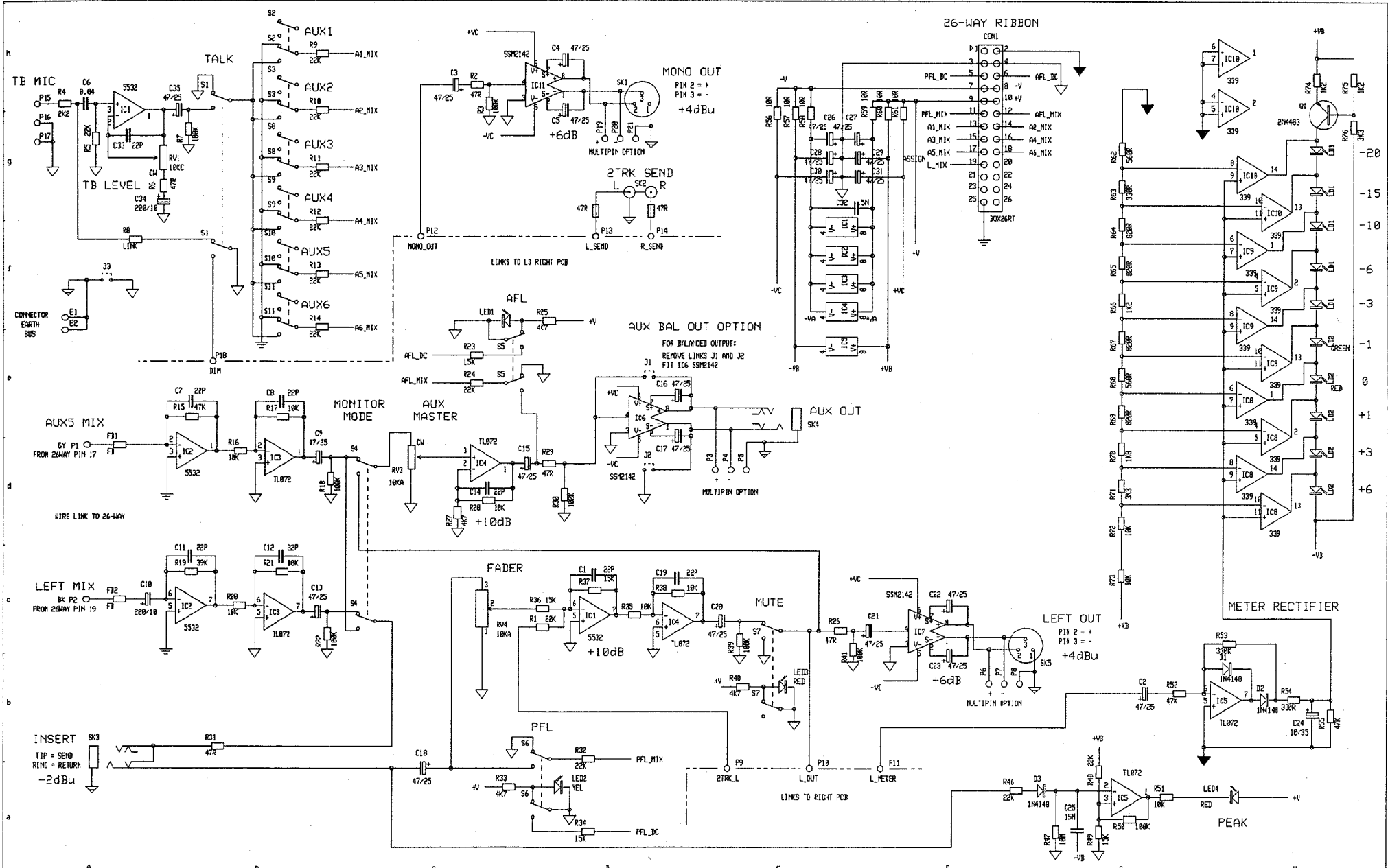
# GROUP

UNIT TITLE
GL3
DRAWING TITLE
GROUP CIRCUIT DIAGRAM PCB TYPE AG0322

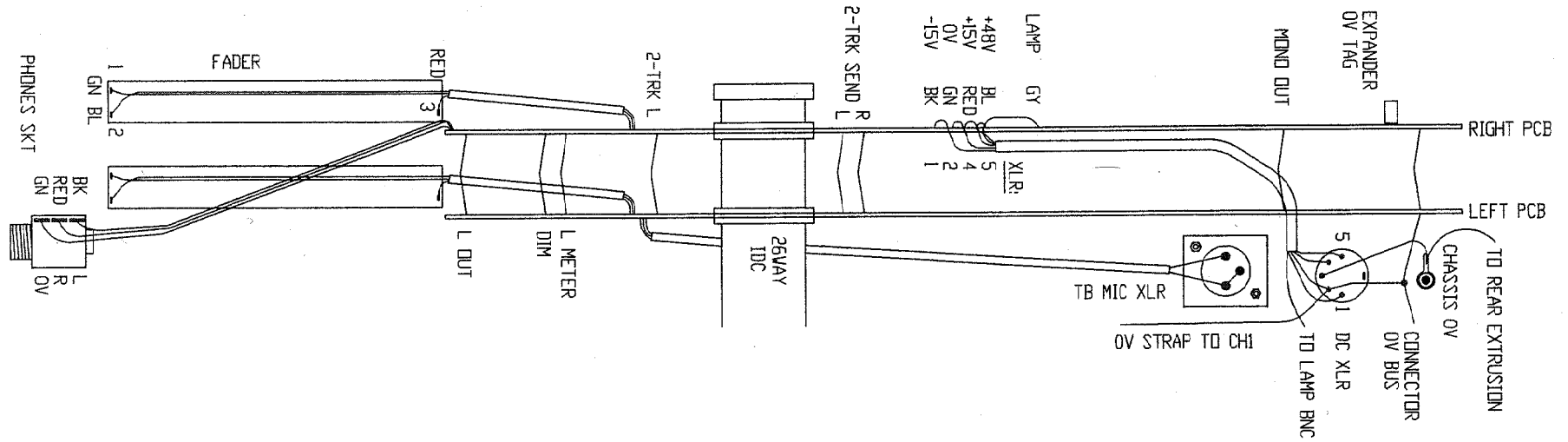
MANUFACTURED IN ENGLAND BY
ALLEN & HEATH
DRAWING No.
D177 ISSUE 2

# MASTER LEFT AND RIGHT

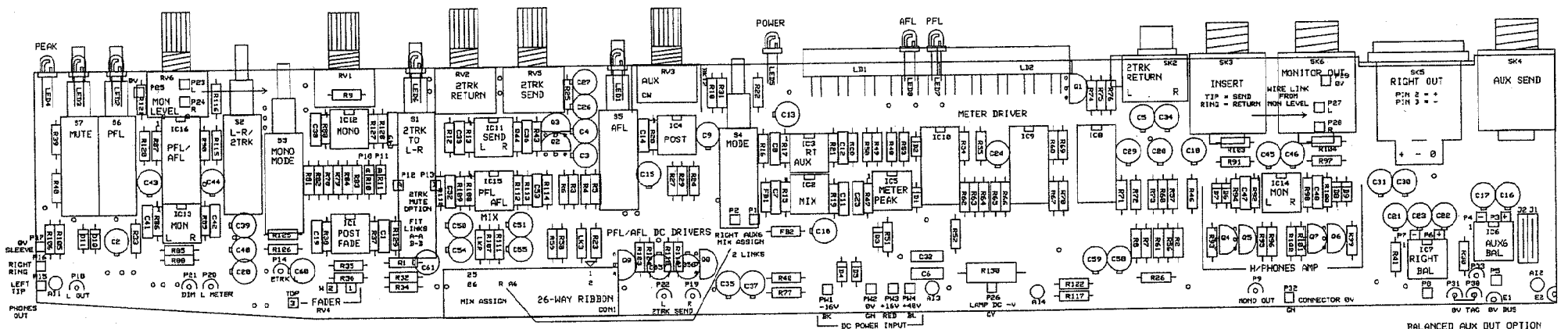




ISS.	REVISION	BY	DATE	NOTES	UNIT TITLE	MANUFACTURED IN ENGLAND BY
P1	ORIGIN	CD	17-7-92	1. RESISTORS MARKED # ARE 1% ALL OTHERS ARE 5% 1/4W UNLESS OTHERWISE MARKED	GL3	ALLEN & HEATH
1	PRODUCTION	CD	30-8-92	2. ELECTROLYTIC CAPACITORS ARE µF/VOLTS	DRAWING TITLE	
2	ICI WAS TL072	DRP	8-12-93		LEFT LEFT CIRCUIT DIAGRAM PCB TYPE AG0323	DRAWING No. D178 ISSUE 2

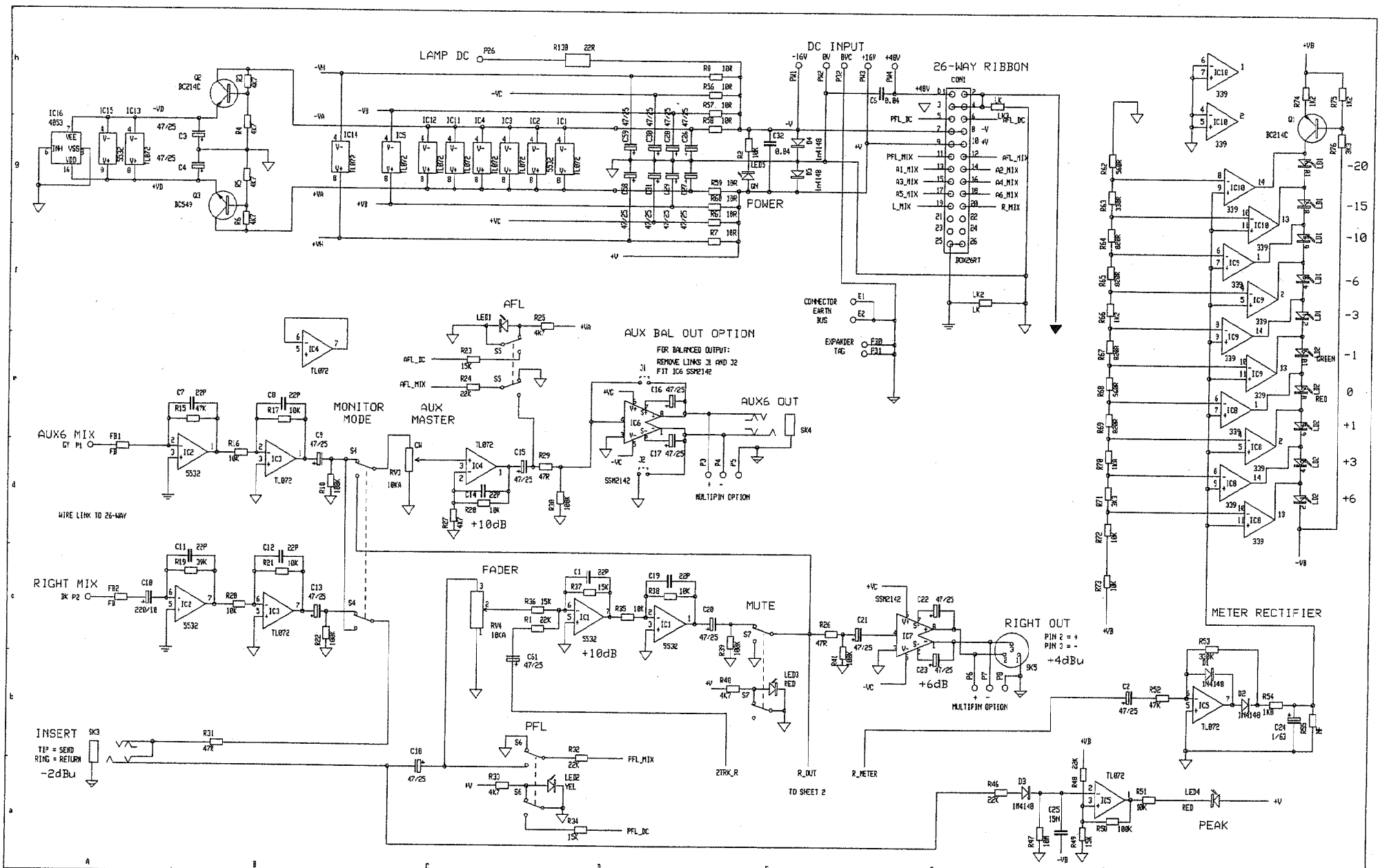


# MASTER WIRING



FH401D GL3 RIGHT PCB AG0324 ISSUE 2 COMPONENT LAYOUT

BALANCED AUX OUTPUT OPTION  
TO FIT BALANCED OUTPUT OPTION  
REMOVE LINKS J1 AND J2  
PLUG IN IC6 55P014E



ISS.	REVISION	BY	DATE	NOTES
1	ORIGIN	CD	19-8-92	1. RESISTORS MARKED # ARE 1% ALL OTHERS ARE 5% 1/4W UNLESS OTHERWISE MARKED 2. ELECTROLYTIC CAPACITORS ARE µF-VOLTS
2	IC1 WAS TL072 R37 WAS 47K	CD	13-10-92	

# RIGHT

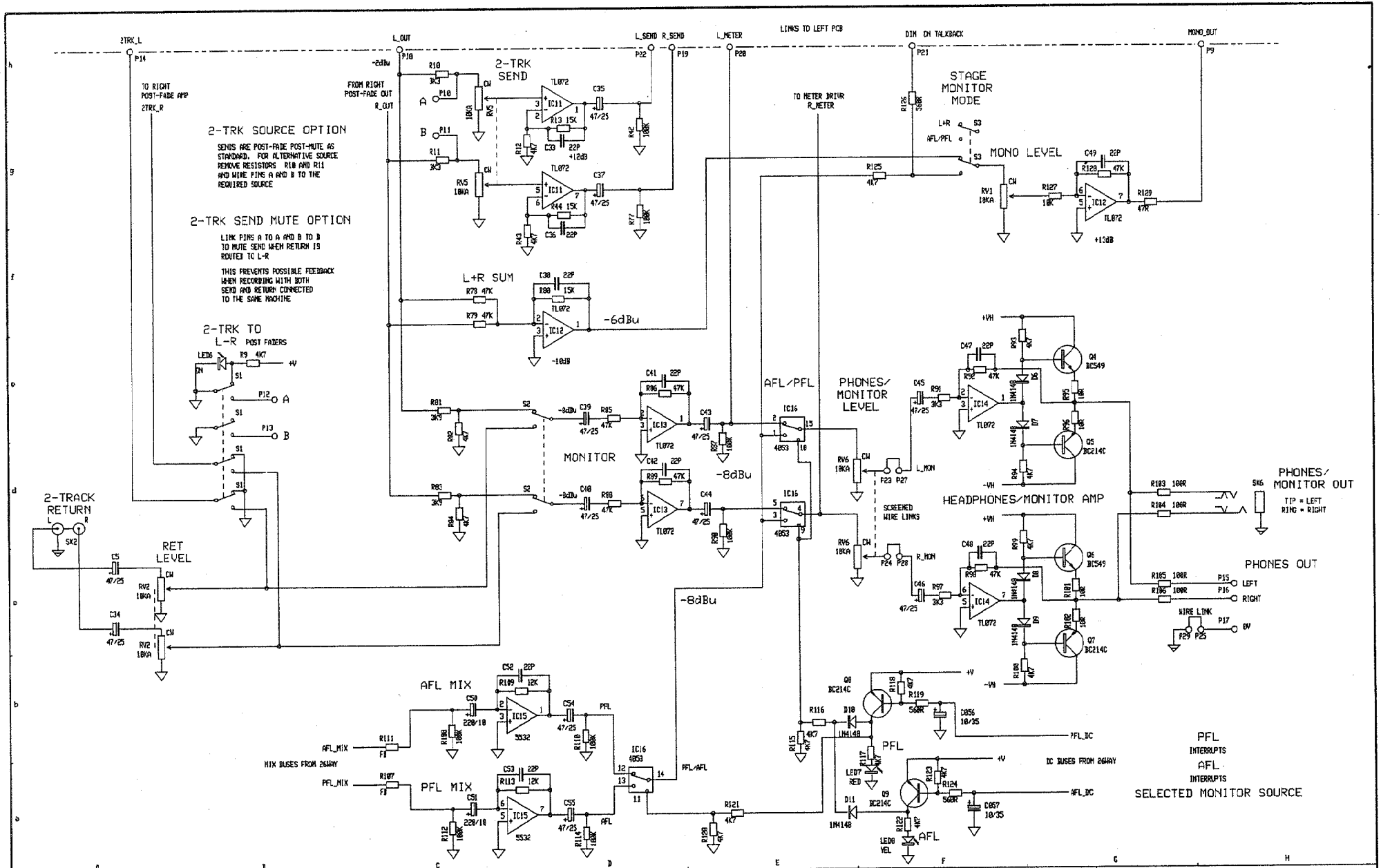
UNIT TITLE  
**GL3** SHEET 1 OF 2

DRAWING TITLE  
**RIGHT CIRCUIT DIAGRAM**  
PCB TYPE AG0324

MANUFACTURED IN ENGLAND BY  
**ALLEN & HEATH**

DRAWING No. **D179** ISSUE 2





**2-TRK SOURCE OPTION**

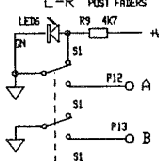
SENDS ARE POST-FADER POST-MUTE AS STANDARD. FOR ALTERNATIVE SOURCE REMOVE RESISTORS R10 AND R11 AND WIRE PINS A AND B TO THE REQUIRED SOURCE

**2-TRK SEND MUTE OPTION**

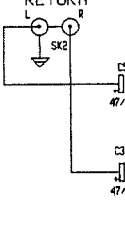
LINK PINS A TO A AND B TO MUTE SEND WHEN RETURN IS ROUTED TO L-R

THIS PREVENTS POSSIBLE FEEDBACK WHEN RECORDING WITH BOTH SEND AND RETURN CONNECTED TO THE SAME MACHINE

**2-TRK TO L-R POST FADERS**



**2-TRACK RETURN**



**RET LEVEL**



ISS.	REVISION	BY DATE	NOTES
P1	ORIGIN	CD 19-8-92	

NOTES

1. RESISTORS MARKED # ARE 1% ALL OTHERS ARE 5% 1/4W UNLESS OTHERWISE MARKED
2. ELECTROLYTIC CAPACITORS ARE #F-VOLTS

RIGHT

UNIT TITLE  
GL3 SHEET 2 OF 2

DRAWING TITLE  
RIGHT CIRCUIT DIAGRAM  
PCB TYPE AG0324

MANUFACTURED IN ENGLAND BY  
ALLEN & HEATH

DRAWING No. D179 ISSUE 1