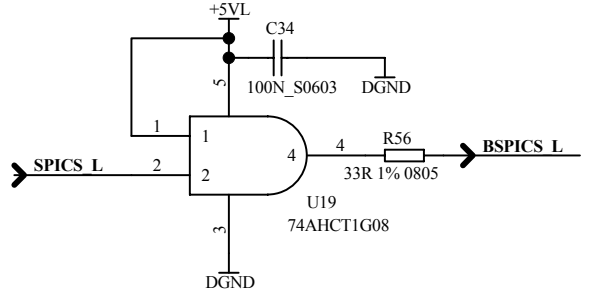
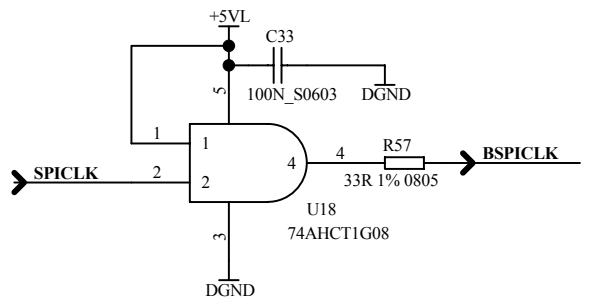
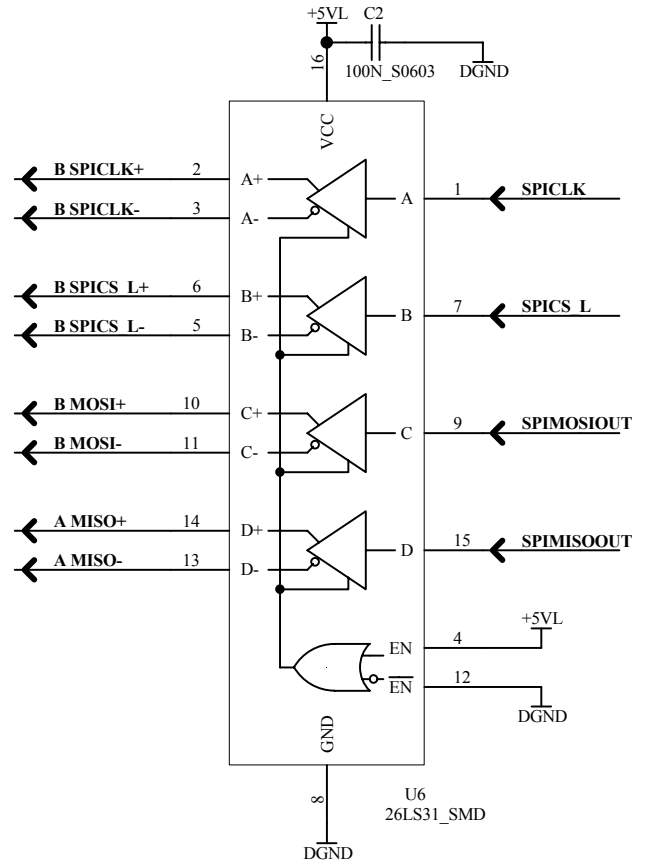
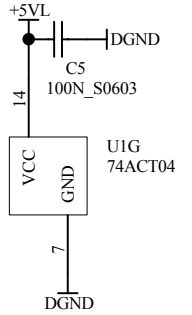
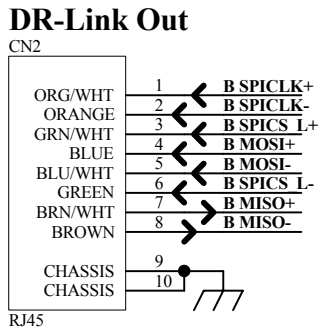
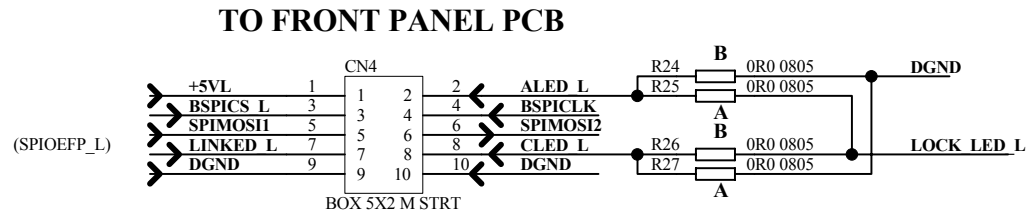
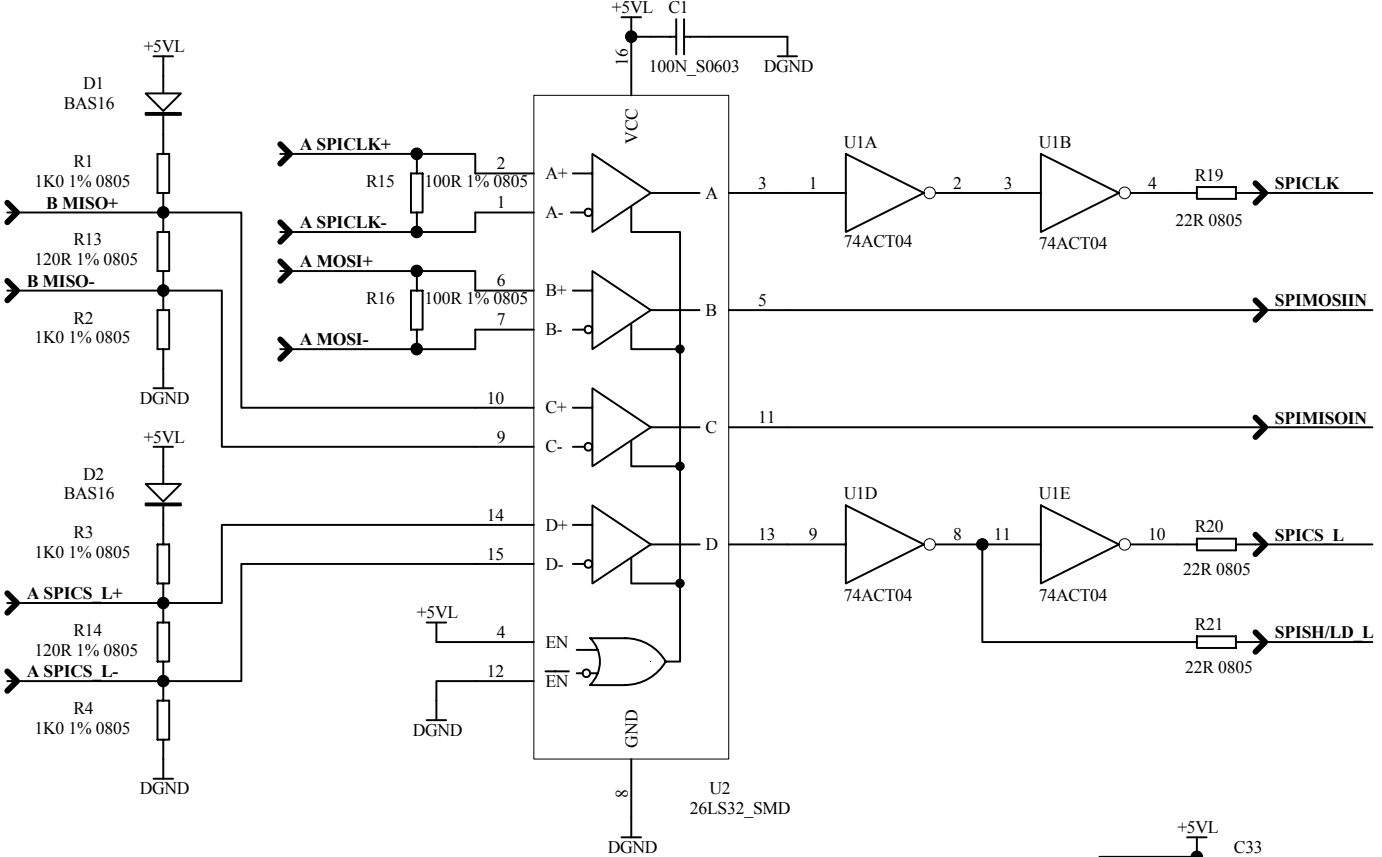
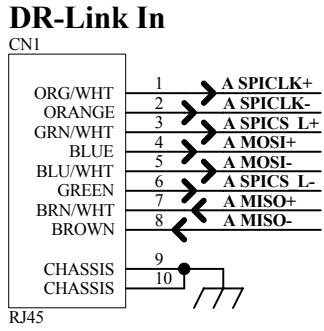
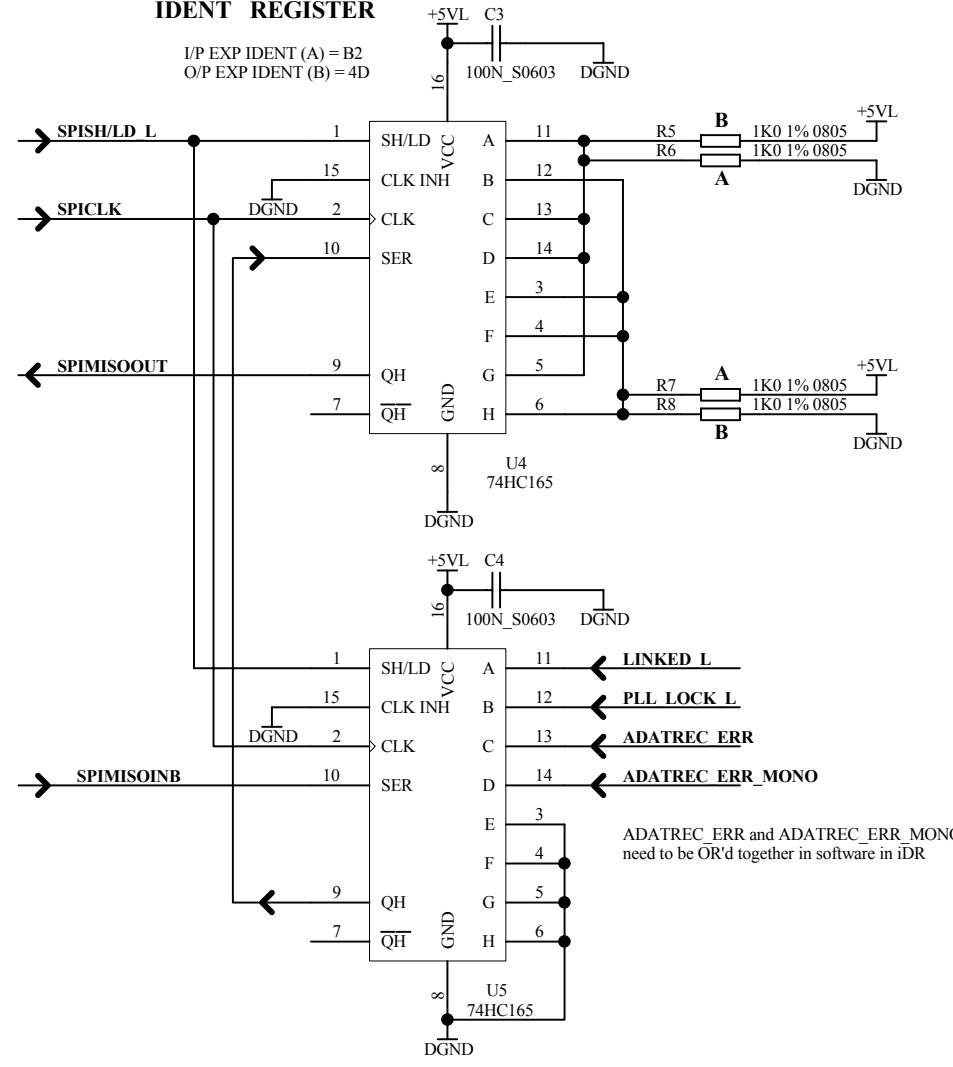


This PCB is used in 2 assys
 Parts marked A are fitted on Input Expander only
 Parts marked B are fitted on Output Expander only
 All other parts are fitted on both
 These characters are in Part Field 1 and hence can be included in BOM generation
 To include on circuit - set hidden fields on and set sheet path and other part fields to blank



IDENT REGISTER

I/P EXP IDENT (A) = B2
 O/P EXP IDENT (B) = 4D



ADATREC_ERR and ADATREC_ERR_MONO need to be OR'd together in software in iDR

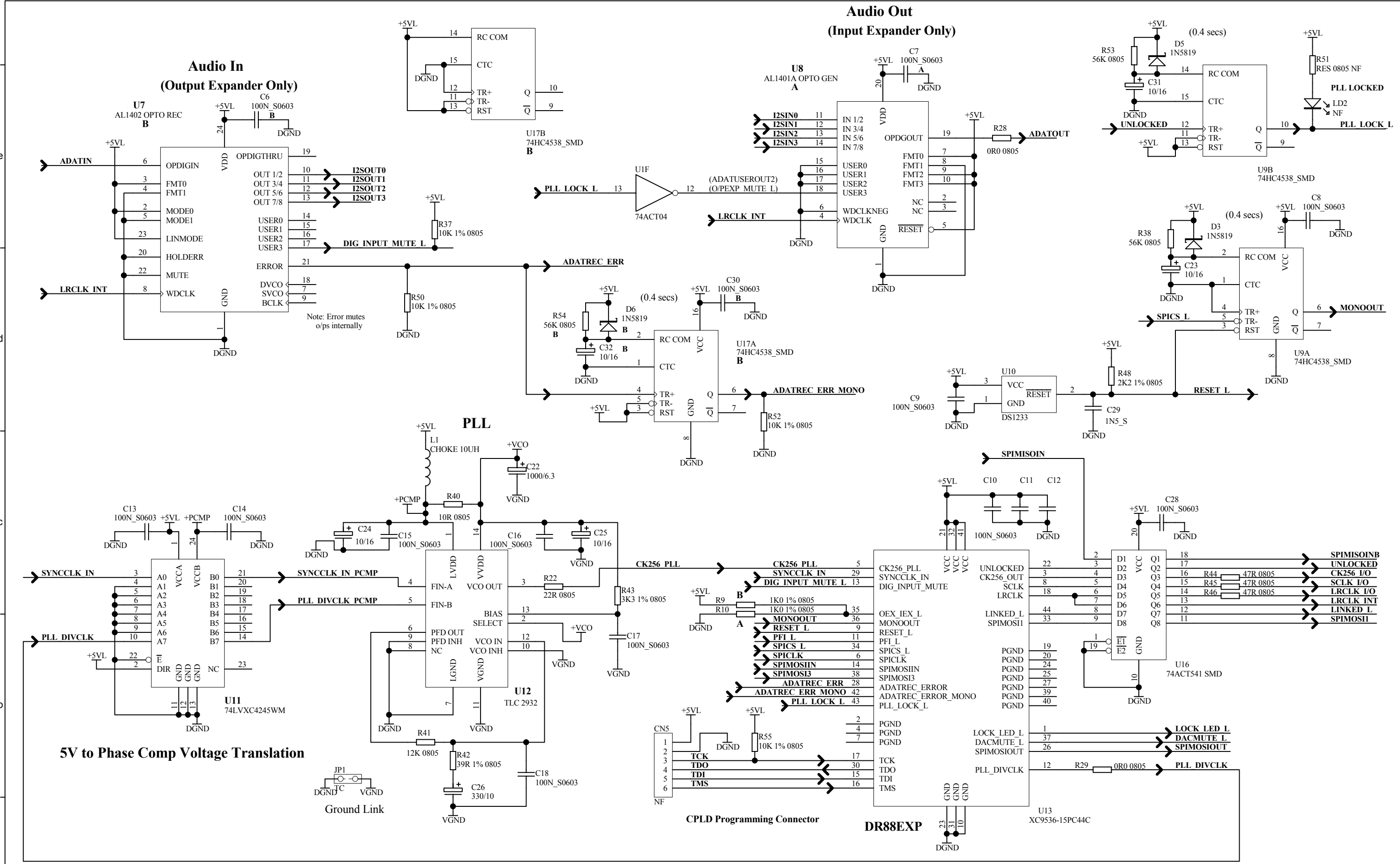
ISSUE	BY	DATE
A	DLP	25/2/02
B	DLP	13/6/02
1	JB	04/9/02

FILE: C4257_1P1.Sch

PRINTED: 16:04:49 19-Feb-2003

TITLE: DR88 EXPANDER COMMS	ISSUE: 1	SHEET: 2 OF 4	A3
PAGE:	DRG No: AG4257		

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 Kernick Industrial Estate,
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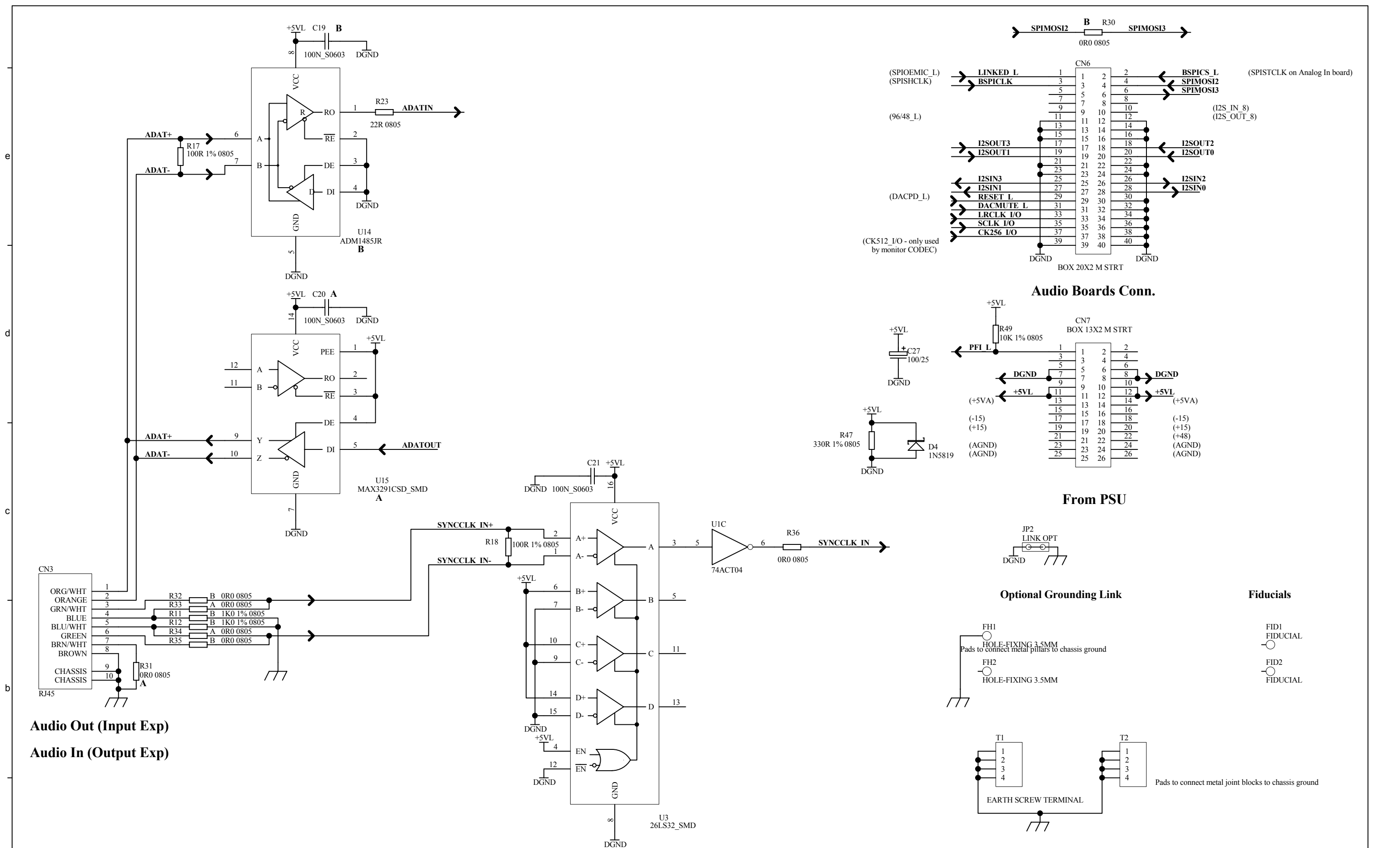


ISSUE	BY	DATE
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I	JB	04/9/02

FILE: C4257_1P2.Sch	PRINTED: 16:04:50 19-Feb-2003
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TITLE: DR88 EXPANDER COMMS	PAGE:
DRG No: AG4257	ISSUE: 1
SHEET: 3 OF 4	A3

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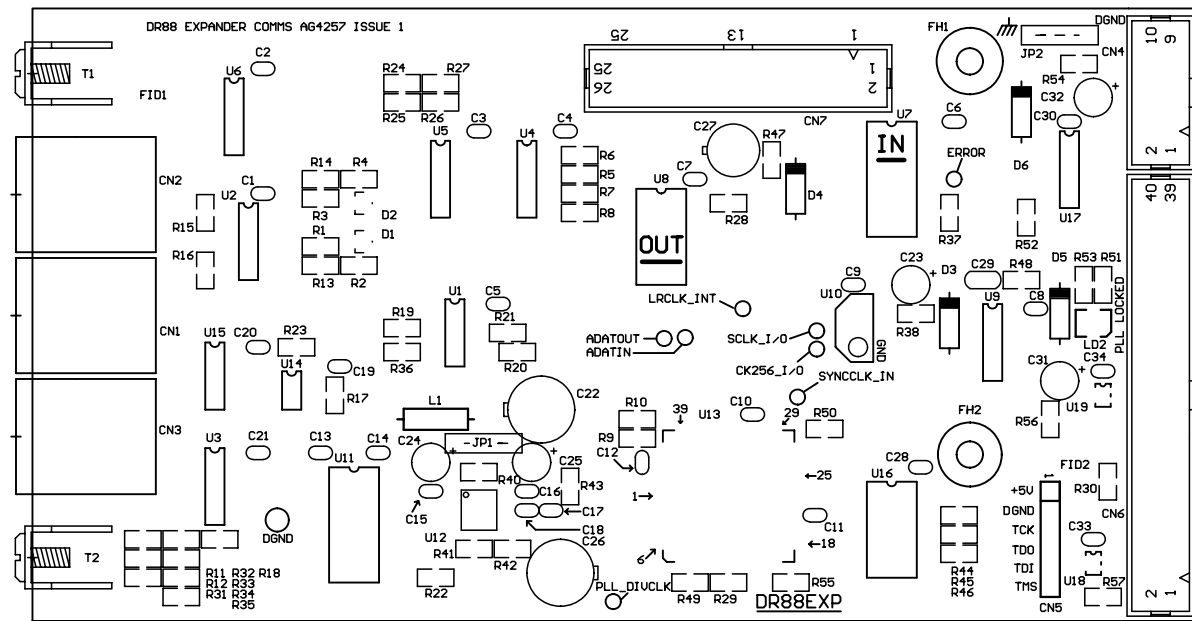


ISSUE	BY	DATE
A	DLP	25/2/02
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1	JB	04/9/02

FILE: C4257_1P3.Sch	PRINTED: 16:04:50 19-Feb-2003
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TITLE: DR88 EXPANDER COMMS	PAGE:
DRG No: AG4257	ISSUE: 1
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TOP OVERLAY

.GTO