Note : MODCK1 & 2 Pulled Up Elsewhere on cct

10 MHz Oscillator

Power On Reset

Battery Back Up VARTA 2/V80H 2.4V 70mAh

Distributed evenly close to MPC850 VDDL pins.

U3

MPC_850

Host Processor

N.B. Chip selects are used as follows:-
0 - FLASH (16-bit)
1 - SRAM
2 - SDRAM
3 - DSP's (Further decoded to 4 lines)
4 - LCD

IP_B0-7 used by PCMCIA if reqd

Debug Port

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Kernick Industrial Estate, Penryn, Cornwall, England. TR10 9LU	A	DLP	18/5/01
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	2	DLP	18/02/03

FILE: C4481_2P2(Host).SCH | PRINTED: 13:44:26 24-Sep-2004

TITLE: iDR CPU
PAGE: HOST

DRG No: C4481 ISSUE: 2 SHEET: 1 OF 7

003-006 iss.2

To use a 128 Mbit SDRAM (MT48LC8M16A2)
Connect A9 and A8 to BA0 and BA1 respectively.
Change MAMR[9..11] from 000 to 001 and
Change MAMR[16..18] from 000 to 001

N.B. A10 on SDRAMs connects to A20 of CPU for Row Address
but used for command word during column addess
hence a GPL is used for this line and controlled by UPM

A9/A10 from CPU used as bank select and is MSB of DRAM address.
Must be constant during row and column addressing and not subject to multiplexer

A[8..A31]

SDRAM

U4
MT48LC4M16A2

SDRAM - 64Mbit (4M X 16bit words)

Flash

U5
AM29LV160BB-90 SMD

16-bit flash supports 16 bit access only
Flash - 16Mbit (1M x 16bit Words)

D[0..D15]

Battery Backed SRAM

U7
BS62LV1024SC-70 (SOP-32)

SRAM - 128KBytes (128K X 8 bit words)

These terminating component should be close to TX+ & Tx-.

The traces above should be routed as differential pairs with Z=100 ohm and length < 25mm

The area of the board around the Rx and Tx signals should be kept clear of digital signals.

U6
AM79C874

Ethernet Phy

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2	DLP	18/02/03

FILE: C4481_2P3(Memory_and_Ethernet).SCH

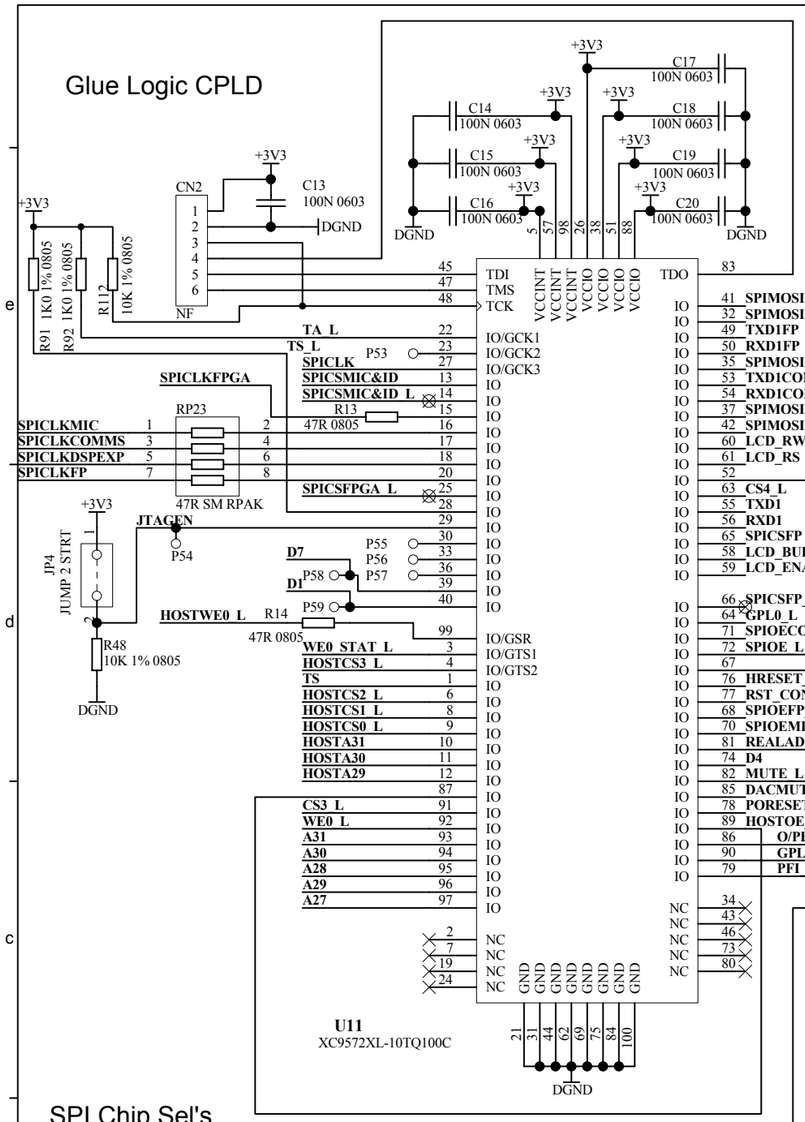
PRINTED: 13:44:26 24-Sep-2004

TITLE: iDR CPU
PAGE: Memory & Ethernet

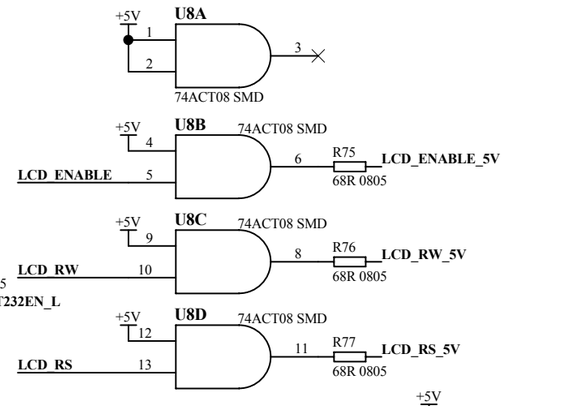
DRG No: C4481 ISSUE: 2 SHEET: 2 OF 7

003-006 iss.2

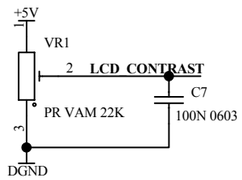
Glue Logic CPLD



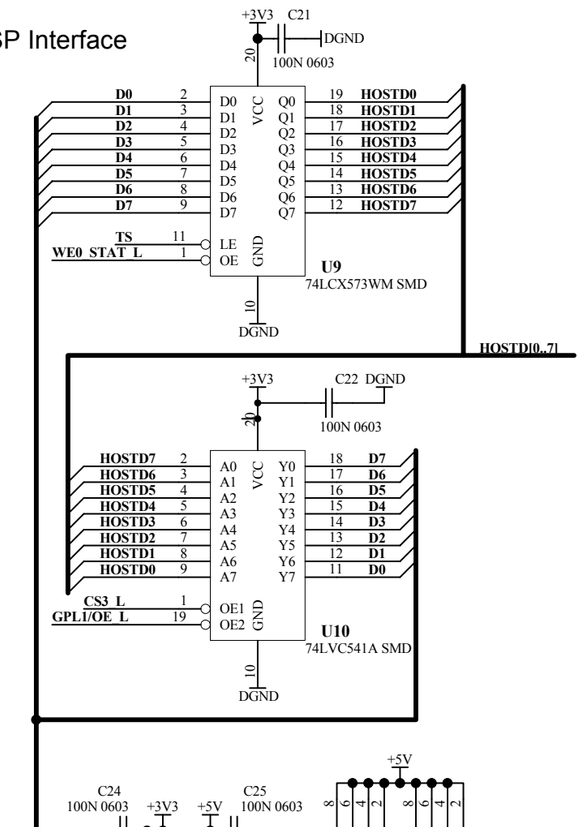
LCD Control Signal Level Conversion



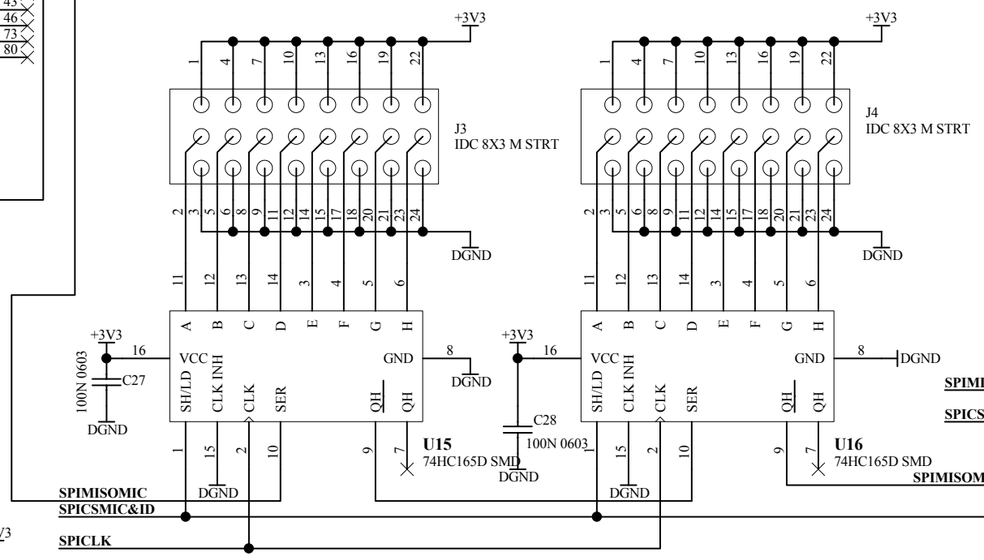
LCD Contrast



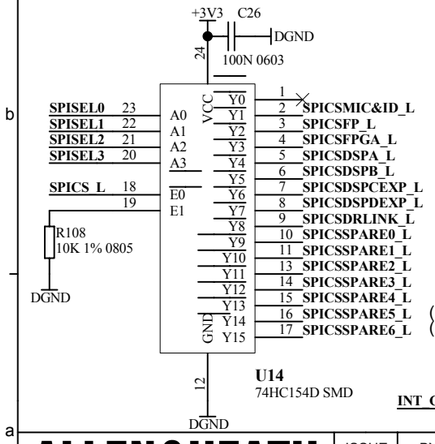
Host / DSP Interface

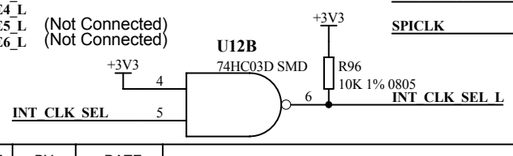


Ident Register

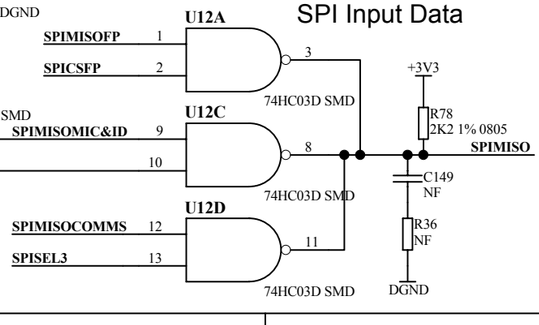


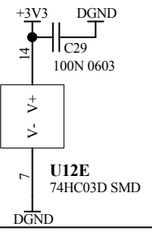
SPI Chip Sel's





SPI Input Data





5V Level Conversion for LCD data

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FILE: C4481_2P4(Glue).SCH | PRINTED: 13:44:27 24-Sep-2004

TITLE: iDR CPU
PAGE: Glue Logic

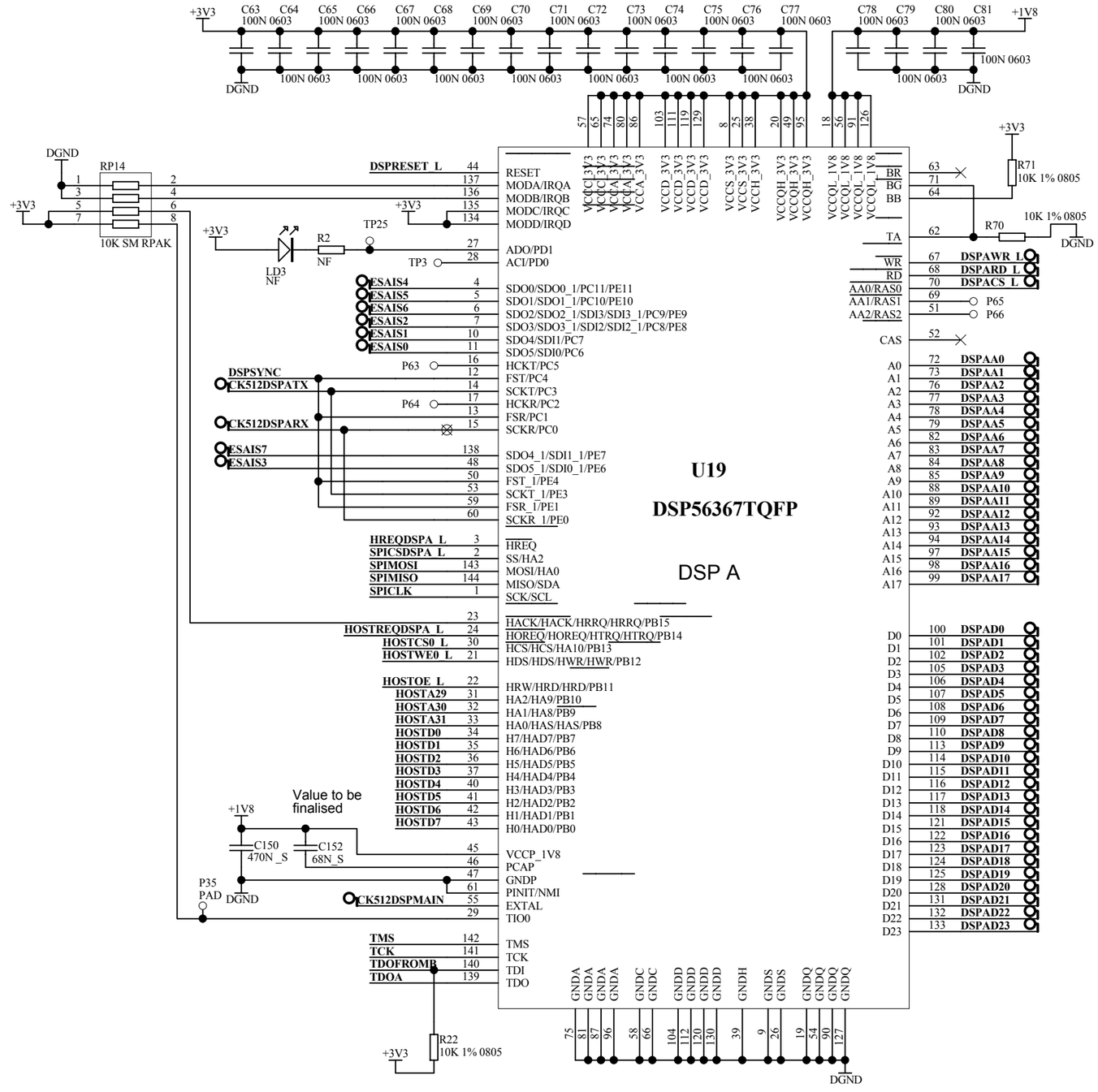
DRG No: C4481 ISSUE: 2 SHEET: 3 OF 7

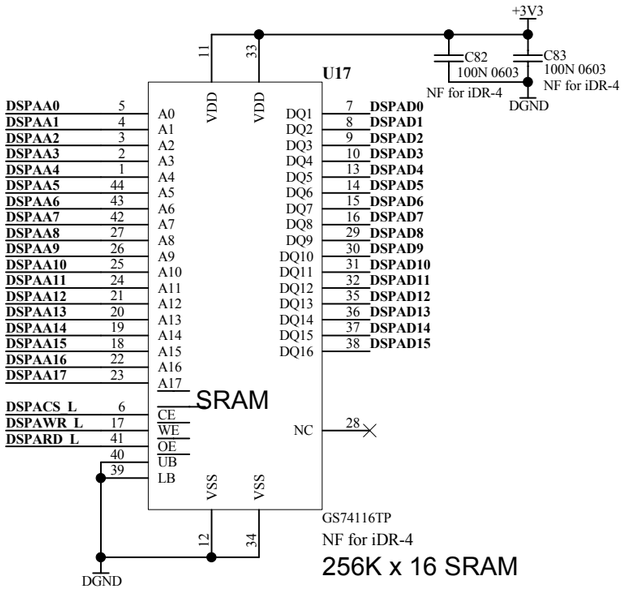
003-006 iss.2

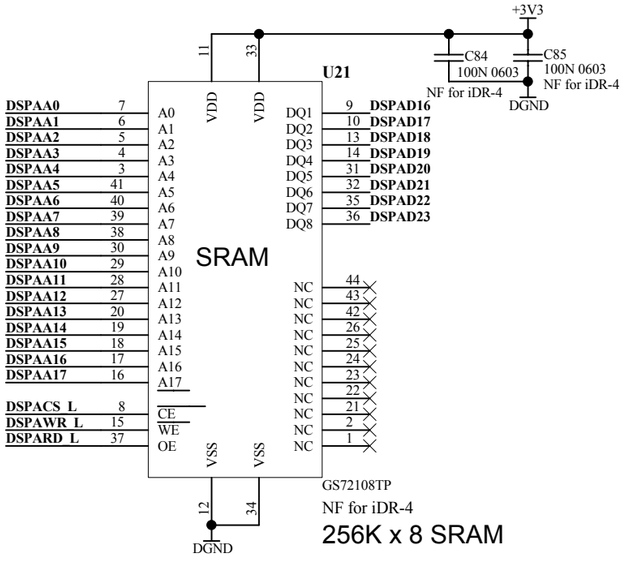
Note SRAM and associated decouplers not fitted for DSP A for iDR-4

This info. is contained in Part Field 1 and hence can be included in BOM generation

(To include on circuit - set hidden fields on and set sheet path and other part fields to blank)







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A	DLP	18/5/01
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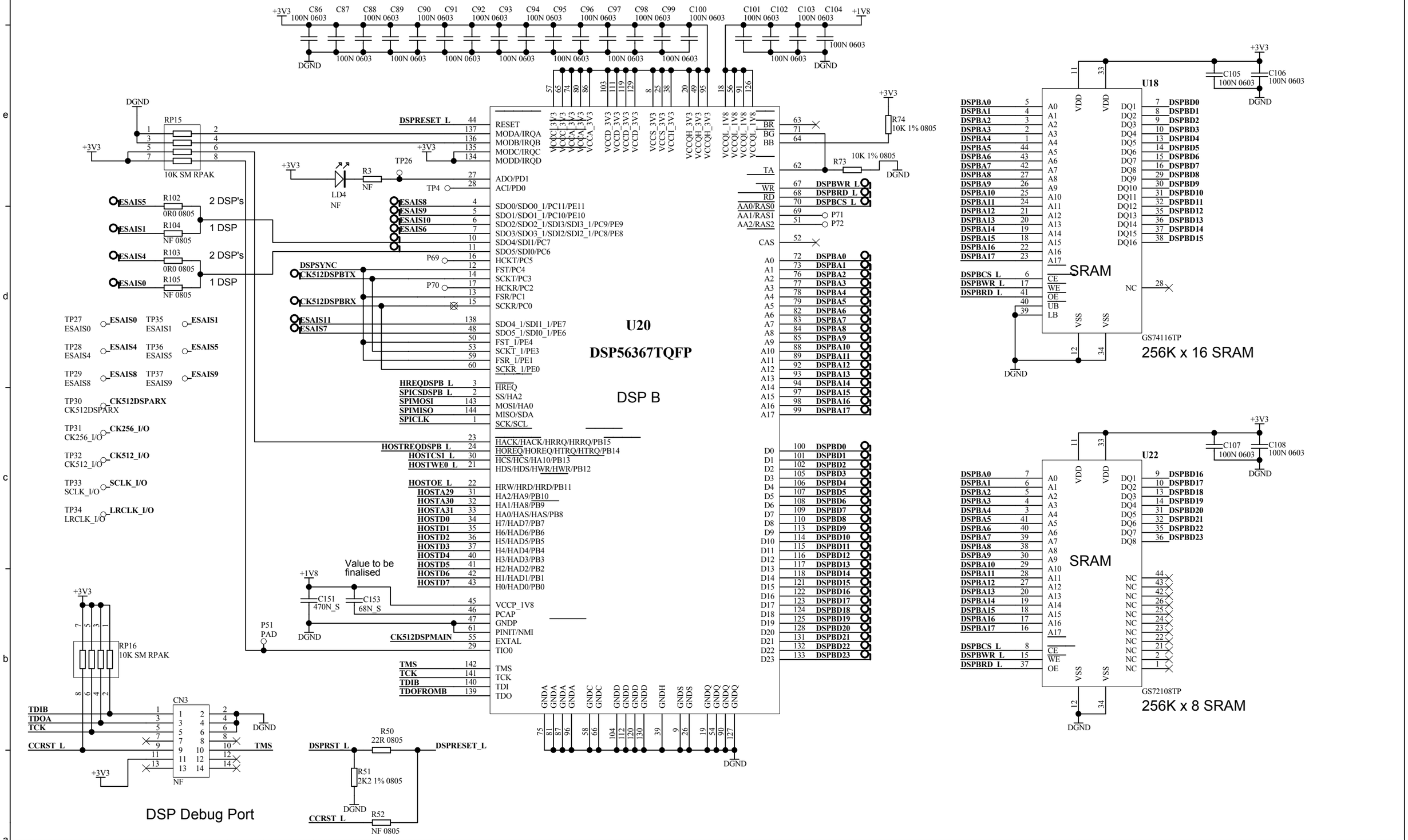
FILE: C4481_2P5(DSP A).SCH

PRINTED: 13:44:27 24-Sep-2004

TITLE: iDR CPU
PAGE: DSP A

DRG No: C4481 ISSUE: 2 SHEET: 4 OF 7

003-006 iss.2



ALLEN&HEATH	TITLE: iDR CPU	
Kernick Industrial Estate, Penryn, Cornwall, England. TR10 9LU	PAGE: DSP B	
Tel: +44 (0)8707 556250 Fax: +44 (0)8707 556251	DRG No: C4481 ISSUE: 2 SHEET: 5 OF 7	

ISSUE	BY	DATE
A	DLP	18/5/01
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2	DLP	18/02/03

FILE: C4481_2P6(DSP B).SCH PRINTED: 13:44:28 24-Sep-2004

003-006 iss.2

Digital Expansion In

U23 — AL1402 OPTO REC

ADATIN, ADATREC_HOLDERR_5V, LRCLK_INT_5V

OPDIGIN, FMT0, FMT1, MODE0, MODE1, LINMODE, HOLDERR, MUTE, WDCLK, VDD, GND, OPDIGTHRU, OUT 1/2, OUT 3/4, OUT 5/6, OUT 7/8, USER0, USER1, USER2, USER3, ERROR, DVCO, SVCO, BCLK

I2SIN4, I2SIN5, I2SIN6, I2SIN7, ADATUSERIN2_5V, DIG_INPUT_MUTE_L

C109 100N 0603

R93 NF, ERROR, LD5 NF, ADATREC_ERROR

Digital Expansion Out

U24 — AL1401A OPTO GEN

I2SOUT4_5V, I2SOUT5_5V, I2SOUT6_5V, I2SOUT7_5V, ADATUSEROUT2_5V, O/PEXP_MUTE_5V_L, LRCLK_INT_5V

IN 1/2, IN 3/4, IN 5/6, IN 7/8, OPDGOUT, FMT0, FMT1, FMT2, FMT3, USER0, USER1, USER2, USER3, WDCLKNEG, WDCLK, NC, RESET

R15 0R0 0805 ADATOUT

R109 10K 1% 0805

C110 100N 0603

Delay Line

U25 DS1033Z-10

CK512DSPARXPRE, CK512DSPBTX, CK512DSPATX

IN1, IN2, IN3, OUT1, OUT2, OUT3, VCC, GND

CK512DSPARX, CK512DSPCRX_EXP, CK512DSPBRX

C111 C112 C113 C114 C115 C116 C117 C118 100N 0603

Internal Audio Oscillator

U27 — OSC-24.576M-SMD

INT_CLK_SEL, ENABLE, VCC, GND, OUT

C123 100N 0603, R79 22R 0805

U32E 74HCT08, C54 100N 0603

PLL

U28, L3 CHOKE NF, L2 CHOKE 10UH, R67 1K0 1% 0805, C121 NF, C139 NF, C122 NF, VCO, JP2 10R, C154 1000/6.3, C140 10/16, C126 100N 0603, C127 100N 0603, C141 10/16

U30 TLC 2932

FIN-A, FIN-B, VCO OUT, BIAS SELECT, PFD OUT, PFD INH, NC, VCO IN, VCO INH, LVDD, VVDD, LGND, VGND

CK512_PLL, R82 22R 0805, R83 3K3 1% 0805, C128 100N 0603, R24 10K 1% 0805, R23 12K 0805, R8 22R 0805, C129 100N 0603, C157 330/10

R97 10K 1% 0805, Q3 BC848B, INT_CLK_SEL_L

PROGD, LD8 NF, R49 NF 0805, R72 10K 1% 0805, R106 10K 1% 0805, R107 10K 1% 0805, TP22, TP23, TP24

FPGA

I2SIN0–I2SIN8, I2SOUT0–I2SOUT8, RP24 47R SM RPAK, RP25 47R SM RPAK, R17 47R 0805

CK512_OSC, CK512_PLL, INT_CLK_SEL, SYNCCLK_IN, 96/48K, SPARE I/O, ADATUSERIN2_5V, ADATUSERIN2, PROGGED, INIT, DOUT, CCLK, DONE, DIN, PROGRAM, M1, M0

TP38 SYNCCLK_IN, 96/48_L, FPGA_SPARE1, FPGA_SPARE2, FPGA_SPARE3, TP5, TP6, TP7

R84 4K7 1% 0805, FPGAINIT_L, XILADOUT, CCLK, DONE, DIN, PROG_L, CN4 NF

R86 4K7 1% 0805, C158 330P 0603

SPICLKFPGA R57 0R0 0805, FPGADONE R58 0R0 0805, SPIMOSI R59 0R0 0805, FPGAPROG_L R60 0R0 0805

DTODSPAI0, DTODSPAI1, R81 33R 1% 0805, R80 33R 1% 0805, ESAIS0, ESAIS1

DFROMDSPBO0–3, ESAIS8–11

DFROMDSPEXPO0–3, ESAIE0–3

DTOEXTRA1–3, DSPSYNC_EXTRA, RP26, RP27, RP28, RP29 47R SM RPAK

ESAIEXTRAOUT1–3, DSPSYNC_EXTRA, CK512_EXTRA, CK512DSPMAIN, DSPSYNC, CK512DSPATX, CK512DSPBTX, CK512DSPARXPRE, DSPSYNC_EXP, CK512DSPMAIN_EXP, CK512DSPCTX_EXP, CK512DSPDTX_EXP, LRCLK_EXP, SYNCCLK_OUT

LRCLK_I/O, SCLK_I/O, CK256_I/O, CK512_I/O, PLL_LOCK, FRAME_CLK, FPGA_WDOG, LRCLK_HOST_1, LRCLK_INT, PLL_DIVCLK, EXPFITTED, EXTRAFITTED, ADATREC_ERROR, ADATREC_ERROR_FRAME, FPGAMUTE_L, PWRDWN, TDI, TDO, TCK, TMS

R98, R99, R100, R101, R54 47R 0805, R19 47R 0805, R95 NF, LOCK, LD7 NF, TP8, TP9, TP10, TP11, TP12, R113 10K 1% 0805, R114 10K 1% 0805

U31 XCS05XL-4VQ100C

3V3 to 5V Translation

C124 100N 0603, C125 100N 0603

U29 74LVXC4245WM SMD

SYNCCLK_IN, PLL_DIVCLK, SYNCCLK_PCMP, SYNCCLK_IN, PLL_DIVCLK_PCMP, LRCLK_INT_5V, LRCLK_INT

R55 0R0 0805 NF, R37 NF, R56 0R0 0805, R38 NF, R39 NF, R111 10K 1% 0805

5V to Phase Comp Voltage Translation

U26 — 74ACT541 SMD

C120 100N 0603

ADATREC_HOLDERR, O/PEXP_MUTE_L, ADATUSEROUT2, LRCLK_INT

ADATREC_HOLDERR_5V, O/PEXP_MUTE_5V_L, ADATUSEROUT2_5V, LRCLK_INT_5V

R16 47R 0805, R110 10K 1% 0805

RP4 10K SM RPAK

LRCLK_HOST_1, 96/48_L, ADATUSERIN2, ADATUSEROUT2

Ground Link

JP1 JC

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FILE: C4481_2P7(FPGA).SCH

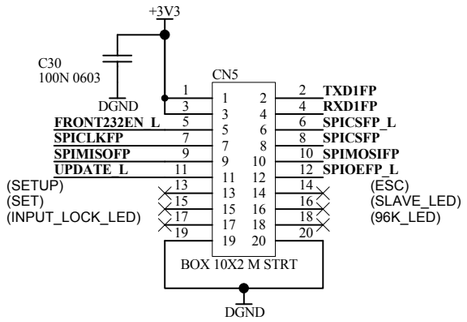
PRINTED: 13:44:28 24-Sep-2004

TITLE: iDR CPU

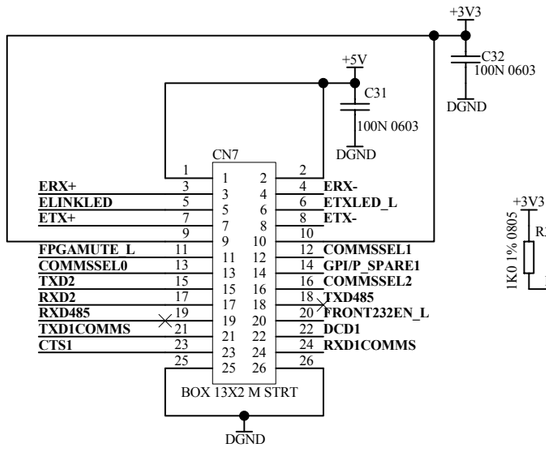
PAGE: FPGA and Audio Interface

DRG No: C4481 ISSUE: 2 SHEET: 6 OF 7

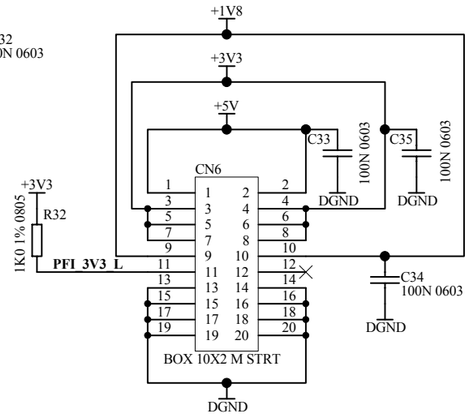
003-006 iss.2



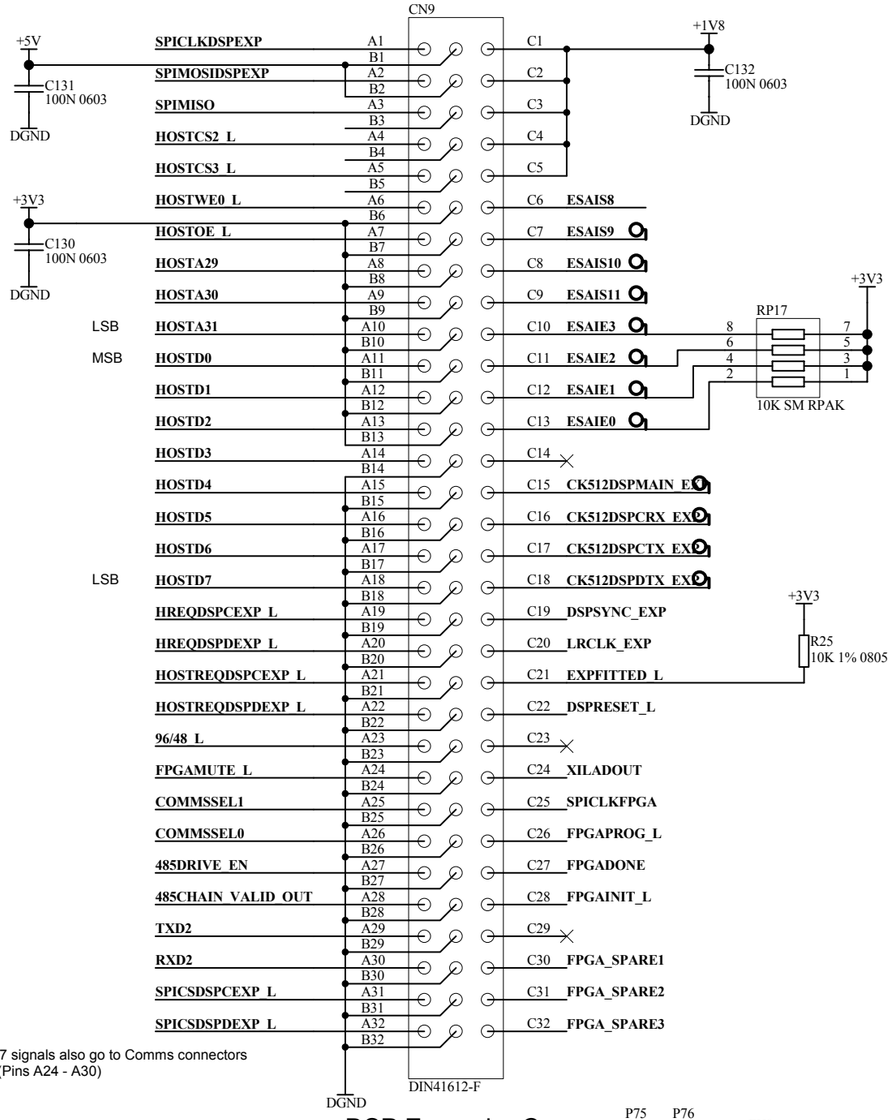
Front Panel Conn.



Comms 1&3 Conn.

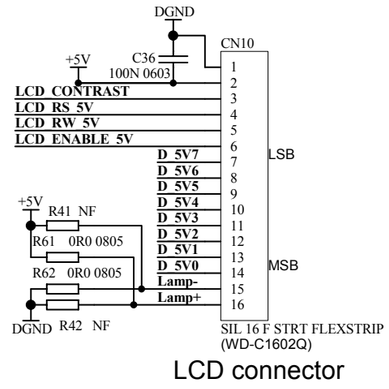


Power Conn.

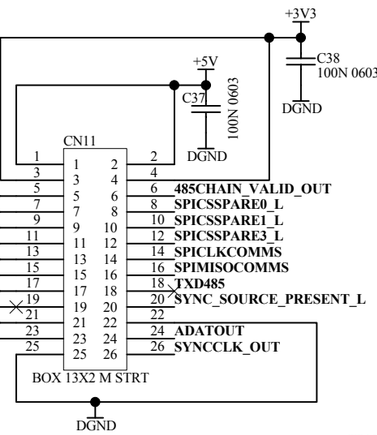


DSP Expander Conn.

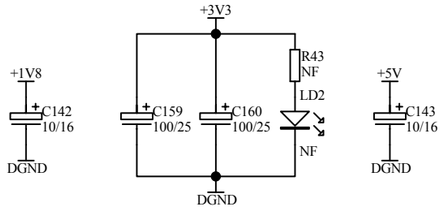
Note : 7 signals also go to Comms connectors
(Pins A24 - A30)

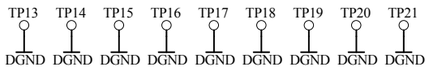


LCD connector

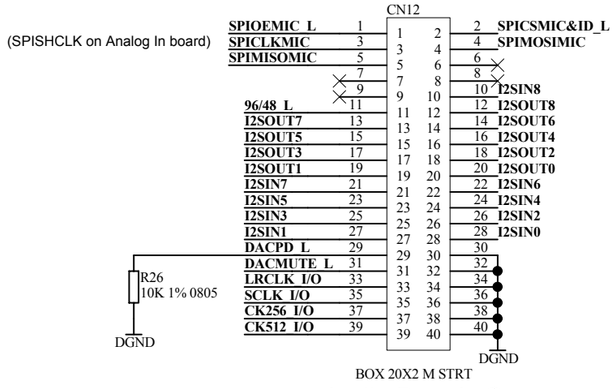


Comms 2&4 Conn.



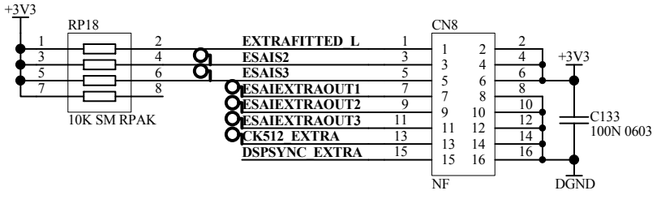


Positioned around PCB for scope grounds

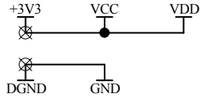


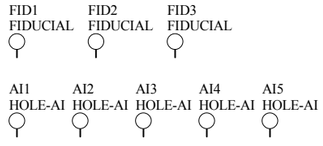
Audio Boards Conn.

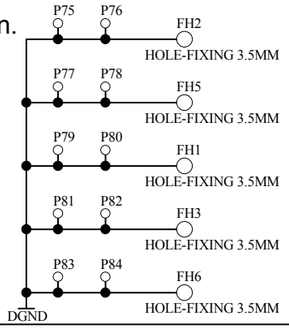
(SPISTCLK on Analog In board)



Extra ESAI's Conn.







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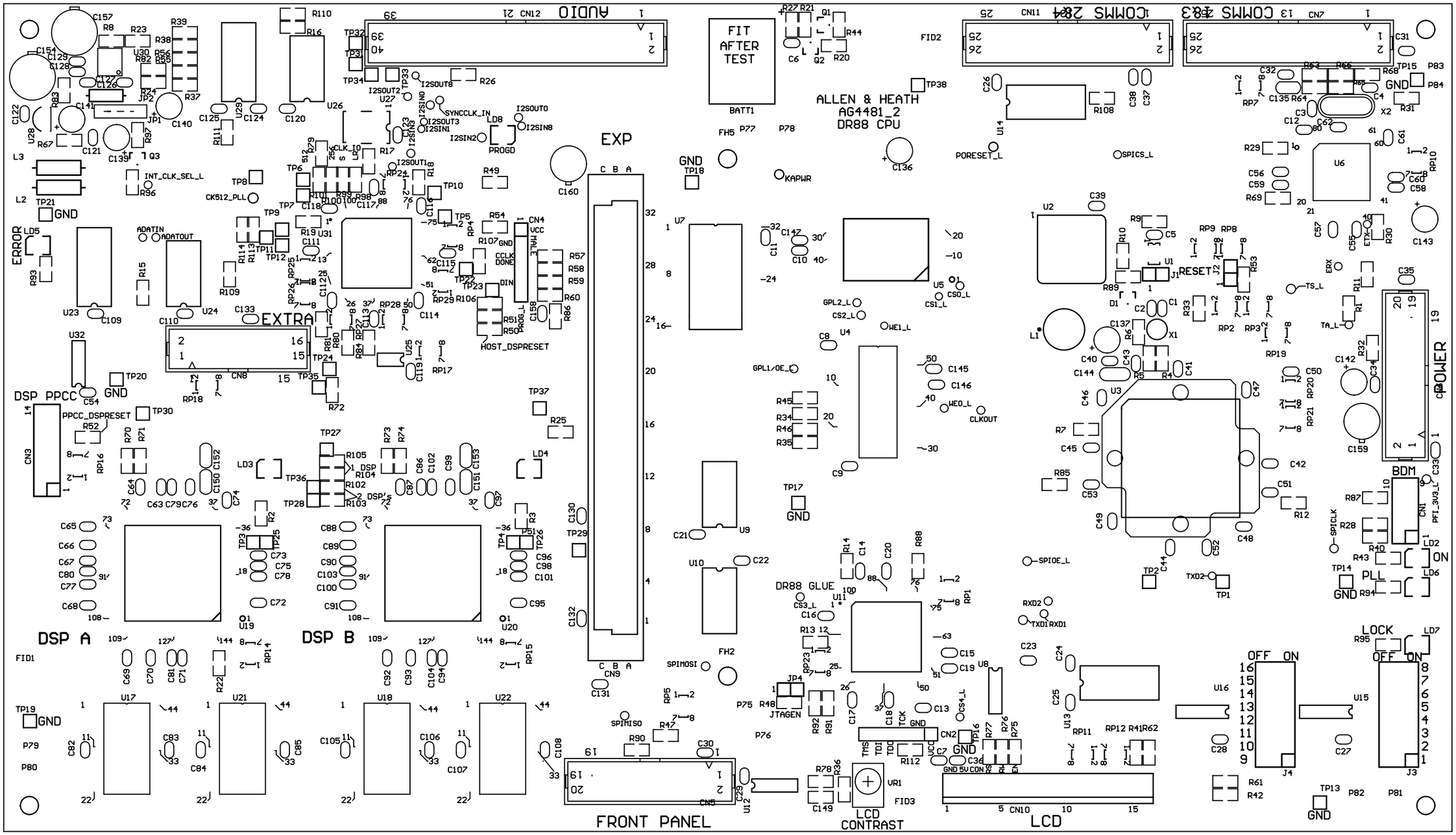
	2	DLP	18/02/03

FILE: C4481_2P8(Connectors).SCH | PRINTED: 13:44:29 24-Sep-2004

TITLE: iDR CPU
PAGE: Connectors

DRG No: C4481 ISSUE: 2 SHEET: 7 OF 7

003-006 iss.2


AUDIO
COMMS 284
COMMS 283
FIT AFTER TEST
ALLEN & HEATH
AG4481_2
DR88 CPU
EXP
EXTRA
DSP PPCC
DSP A
DSP B
DR88 GLUE
FRONT PANEL
LCD CONTRAST
LCD
POWER
RESET
BDM
PLL
LOCK
ON
OFF ON
ERROR
GND
HOST_DSPRESET
PPCC_DSPRESET
INT_CLK_SEL_L
CK512_PLL
ADATIN
ADATOUT
SYNCCLK_IN
PROGD
KAPWR
PORESET_L
SPICS_L
SPIOE_L
SPIMOSI
SPIMISO
SPICLK
JTAGEN
TXD1
RXD1
TXD2
RXD2
CLKOUT
TS_L
TA_L
ETX
ERX
PFI_3V3_L
BATT1
FH5
FH2
FID1
FID2
FID3
CN1
CN2
CN3
CN4
CN5
CN7
CN8
CN9
CN10
CN11
CN12
J1
J2
J3
J4
X1
X2
VR1
JP1
JP2
JP4
LD2
LD3
LD4
LD5
LD6
LD7
LD8
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
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U27
U29
U30
U31
U32
P75
P76
P77
P78
P79
P80
P81
P82
P83
P84

003-006 iss.2